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SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 1/17/03 Serial # 09/862,827 Priority Application Date 11/3/00

Your Name [illegible] Examiner #

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01-17-03 P03:07 IN

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Claims 53-59

Problem: See Page 1 lines 17-33
" 2 " 1-14

Solution: " " 3 " 6-25

stringer unwanted fragments of polysilicon that can be a source for a short if not removed prior to finalization of the device

Staff Use Only

Searcher: Derrick Balick

Searcher Phone:

Searcher Location: STIC-EIC2800, CP4-9C18

Date Searcher Picked Up: 1/21/03

Date Completed: 1/21/03

Searcher Prep/Rev Time:

Online Time:

Type of Search

Structure (#)

Bibliographic

Litigation

Fulltext

Patent Family

Other

Vendors

STN ✓

Dialog ✓

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WWW/Internet

Other

6954 110974

SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800

Rev. 8/27/01 This is an experimental format -- Please give suggestions or comments to Jeff Harrison, CP4-9C18, 306-5429.

Date 12/24/03 Serial # 09/162,827 Priority Application Date 11/3/00

Your Name M. Lewis Examiner #

AU 2892 Phone 305-3943 Room Plaza 3-3809

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Circle: USPT DWPI EPO Abs JPO Abs IBM TDB

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What types of references would you like? Please checkmark:

Primary Refs ___ Nonpatent Literature ___ Other ___

Secondary Refs ___ Foreign Patents ___

Teaching Refs ___

What is the topic, such as the **novelty**, motivation, utility, or other specific facets defining the desired **focus** of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

Claims 53-79

Problem: See Page 1 lines 19-33
" " 2 " 1-14
Solution: " " 3 " 6-25

stringers unwanted fragments of polysilicon that can be a source

BEST AVAILABLE COPY

20/9/21
DIALOG(R)File 2:INSPEC

6181691 INSPEC Abstract Number: B1999-04-1265D-027
Title: Chip level reliability on SOI **embedded** memory
Author(s): Kim, Y.-G.; Kim, I.-K.; Park, K.-C.; Lee, S.-I.; Park, J.-W.
Author Affiliation: Semicond. Bus., Samsung Electron. Co. Ltd., Kyungki-Do, South Korea
Conference Title: 1998 IEEE International SOI Conference Proceedings (Cat No.98CH36199) p.135-6
Publisher: IEEE, New York, NY, USA
Publication Date: 1998 Country of Publication: USA xi+174 pp.
ISBN: 0 7803 4500 2 Material Identity Number: XX-1998-02834
Conference Title: 1998 IEEE International SOI Conference Proceedings
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 5-8 Oct. 1998 Conference Location: Stuart, FL, USA
Language: English Document Type: Conference Paper (PA)
Treatment: Practical (P); Experimental (X)
Abstract: In modern DRAM products, stacked-capacitor (STC) cells are widely utilized because the STC cell structure has the advantage of easy fabrication of the storage capacitors. Meanwhile, the drawback of STC cells is the increasing difficulty of the back-end process with each DRAM generation due to the high contact hole aspect ratio resulting from the step height difference between the peripheral **circuit** regimes and **memory array** regimes. This paper describes a novel stacked-capacitor cell structure with a simple wiring process which utilizes the virtual flat surface at the bottom of SOI stacked-capacitor cells. The virtual flat surface is made into a real surface by reversing the capacitor and polishing the substrate with bonded-SOI technology (Nishihara et al. 1992). This memory cell is named an **embedded** memory SOI process (EMSP)(Kim et al. 1996). In this paper, we analyze the problems of capacitor formation under an SOI structure, and confirm the process limitations to improve the **embedded** memory SOI process, using a 16 Mb SOI DRAM with 0.35 mu m design rule technology. We have previously reported the basic EMSP. We focus here on chip-level reliability issues for EMSP memory cell structures and present some solutions. (3 Refs)
Subfile: B
Descriptors: capacitors; **DRAM chips**; **embedded** systems; integrated **circuit** reliability; integrated **circuit** testing; polishing; silicon-on-**insulator**; wafer bonding
Identifiers: chip level reliability; SOI **embedded** memory; DRAM

20/9/19

DIALOG(R)File 2:INSPEC

6272327 INSPEC Abstract Number: B1999-07-1265D-034

Title: High-performance cell transistor design using metallic **shield embedded shallow trench isolation** (MSE-**STI**) for Gbit generation DRAM's

Author(s): Jai-Hoon Sim; Jae-Kyu Lee; Kinam Kim

Author Affiliation: Semicond. R&D Labs., Samsung Electron., Kyungki, South Korea

Journal: IEEE Transactions on Electron Devices vol.46, no.6 p. 1212-17

Publisher: IEEE,

Publication Date: June 1999 Country of Publication: USA

CODEN: IETDAI ISSN: 0018-9383

SICI: 0018-9383(199906)46:6L.1212:HPCT;1-Y

Material Identity Number: I037-1999-006

U.S. Copyright Clearance Center Code: 0018-9383/99/$10.00

Document Number: S0018-9383(99)04739-5

Language: English Document Type: Journal Paper (JP)

Treatment: Theoretical (T)

Abstract: In this paper, the cell transistor design issues for the Gbit level DRAM's with the **isolation** pitch of less than 0.2 mu m caused by the inverse-narrow-channel effect (INCE) and the neighboring storage-node E-field penetration effect (NSPE) will be discussed. Then we propose novel DRAM cell transistor structure by employing metallic **shield** inside the shallow trench **isolation** (**STI**). As confirmed by three-dimensional (3-D) device simulation results, by suppressing the inverse narrow-channel effect and the neighboring storage-node E-field penetration effect using metallic **shield** inside **STI**, we can obtain reliable cell transistors with low-doped substrate, low junction leakage current and uniform V/sub TH/ a distribution regardless of the active width variation. (10 Refs)

Subfile: B

Descriptors: **DRAM chips; isolation** technology

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  File 315:ChemEng & Biotec Abs 1970-2002/Jun
         (c) 2002 DECHEMA
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S2	11	AU='MANDELMAN J A':AU='MANDELMAN JA'
S3	51	AU='MANDELMAN, J.':AU='MANDELMAN, J.A.'
S4	17	AU='DIVAKARUNI R'
S5	1	AU='DIVAKARUNI, RAMACHANDRA'
S6	36	AU='DIVAKARUNI, R.'
S7	1	AU='DIVAKARUNI, MURTHY S.'
S8	31	AU='RADENS, C. J.':AU='RADENS, CARL JOHN'
S9	58	AU='RADENS C':AU='RADENS, CARL JOHN'
S10	151	S1:S9
S11	12175	(EDRAM? ? OR CDRAM? ? OR (EMBEDDED OR ENHANCE?)()(DRAM? ?) OR EMBEDDEDDDRAM? ? OR DYNAMIC(2N)MEMOR?)
S12	229678	(ENHANCED OR EMEBBED)(W)DYNAMIC()RANDOM()ACCESS()MEMOR? OR EDRAM? ? OR CDRAM? ? OR ((CACHE OR E OR C)()(DRAM? ? OR RANDO-M(2N)MEMOR?)) OR CACHEDRAM? ? OR (EMBEDDED OR ENHANCE()DYNAMI-C(2N)MEMOR?)
S13	10	S10 AND S11
S14	2	S10 AND S12
S15	10	S13 OR S14

15/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7068834 INSPEC Abstract Number: B2001-11-1265D-032
Title: Nitride framed shallow trench isolation (NFSTI) for self-aligned buried strap in high performance trench capacitor DRAM/**eDRAM**
Author(s): Kim, B.; Fukuzaki, Y.; Worth, G.; Nuetzel, J.; Williams, G.; Lee, B.; Takegawa, Y.; Halle, S.; Rupp, T.; Sudo, A.; **Divakaruni, R.**; Srinivasan, R.; Mii, T.; Bronner, G.
Author Affiliation: Semicond. R&D Center, IBM Microelectron., Hopewell Junction, NY, USA
Conference Title: 2001 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers (Cat. No.01TH8517) p.89-92
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA 310 pp.
ISBN: 0 7803 6412 0 Material Identity Number: XX-2001-01381
U.S. Copyright Clearance Center Code: 0 7803 6412 0/2001/$10.00
Conference Title: 2001 International Symposium on VLSI Technology, Systems, and Applications. Proceedings of Technical Papers
Conference Sponsor: Ind. Technol. Res. Inst.; Chinese Inst. Eng.; IEEE Circuits & Syst. Soc.; IEEE Electron Devices Soc.; IEEE Electron Devices Soc. Taipei Chapter; IEEE Solid-State Circuit Soc.; IEEE Taipei Sect.; Ministr. Econ. Affairs; Nat. Sci. Council; Taiwan Semicond. Ind. Assoc
Conference Date: 18-20 April 2001 Conference Location: Hsinchu, Taiwan
Language: English
Abstract: A self-aligned buried strap process is developed, using nitride frame with oxide hard mask in shallow trench isolation (STI). The connection between cell access transistor and storage node electrode is a key process in trench type DRAM fabrication. Typical trench cell capacitor DRAM technology forms the strap connection under Si substrate (Buried Strap) for better surface planarity. Trench based **e-DRAM** has significant advantages due to wafer planarity. As the ground rule shrinks beyond 150 nm, the strap resistance variation is critical due to the overlay sensitivity. A new overlay independent strap formation method is introduced, using nitride framed self-aligned trench isolation process which eliminates any possible parasitic connection between the strap and substrate. Masking material and Si RIE process used in NFSTI formation improves array device characteristics. In addition, NFSTI process improves trench level alignment signal contrast due to a phase shift effect.
Subfile: B

15/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

5484823 INSPEC Abstract Number: B9703-1265D-005
Title: Floating-body concerns for SOI **dynamic** random access **memory** (DRAM)
Author(s): **Mandelman, J.A.**; Barth, J.E.; DeBrosse, J.K.; Dennard, R.H.; Kalter, H.L.; Gautier, J.; Hanafi, H.I.
Author Affiliation: IBM Semicond. Res. & Dev. Center, Hopwell Junction, NY, USA
Conference Title: 1996 IEEE International SOI Conference Proceedings (Cat. No.35937) p.136-7

Publisher: IEEE, New York, NY, USA
Publication Date: 1996 Country of Publication: USA xvi+171 pp.
ISBN: 0 7803 3315 2 Material Identity Number: XX96-03123
Conference Title: 1996 IEEE International SOI Conference Proceedings
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 30 Sept.-3 Oct. 1996 Conference Location: Sanibel Island, FL, USA
Language: English

Abstract: Summary form only given. As operating voltages are reduced it becomes increasingly challenging to write a usable signal into the DRAM storage capacitor because of the nonscalability of threshold voltage, due to the limiting effects of subthreshold slope and substrate sensitivity. Since the maximum wordline voltage is limited by reliability considerations, it is extremely important that the threshold voltage of the DRAM array MOSFET be made as low as possible while meeting the static off-current objective for charge retention. SOI, compared to bulk CMOS, appears attractive for a low-voltage (<2 V) DRAM because its superior subthreshold slope and low substrate sensitivity yield a lower source-follower threshold voltage, resulting in increased logical 1 level to be written for the same operating conditions. However, transient effects of the floating body must be considered when designing for long data retention time and low active power. Although earlier work has considered dynamic retention problems for SOI DRAM during normal read/write operations, simulation results presented in this paper address a transient SOI DRAM leakage mechanism which appears during page mode operation, for both partially and fully depleted designs. Two novel solutions for suppressing the transient leakage mechanism have been investigated.
Subfile: B

15/3,AB/3 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06087105
E.I. No: EIP02287009637
Title: Challenges and future directions for the scaling of **dynamic** random-access **memory** (DRAM)
Author: **Mandelman, Jack A.**; Dennard, Robert H.; Bronner, Gary B.; DeBrosse, John K.; Divakaruni, Rama; Li, Yujun; **Radens, Carl J.**
Corporate Source: IBM Microelectronics Division East Fishkill Facility, Hopewell Junction, NY 12533, United States
Source: IBM Journal of Research and Development v 46 n 2-3 March/May 2002. p 187-212
Publication Year: 2002
CODEN: IBMJAE ISSN: 0018-8646
Language: English
Abstract: Significant challenges face DRAM scaling toward and beyond the 0.10-mum generation. Scaling techniques used in earlier generations for the array-access transistor and the storage capacitor are encountering limitations which necessitate major innovation in electrical operating mode, structure, and processing. Although a variety of options exist for advancing the technology, such as low-voltage operation, vertical MOSFETs, and novel capacitor structures, uncertainties exist about which way to proceed. This paper discusses the interrelationships among the DRAM scaling requirements and their possible solutions. The emphasis is on trench-capacitor DRAM technology. 55 Refs.

15/3,AB/4 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05918059
E.I. No: EIP01436699533
Title: Nitride framed shallow trench isolation (NFSTI) for self-aligned buried strap in high performance trench capacitor DRAM/**eDRAM**
Author: Kim, B.; Fukuzaki, Y.; Worth, G.; Nuetzel, J.; Williams, G.; Lee, B.; Takegawa, Y.; Halle, S.; Rupp, T.; Sudo, A.; **Divakaruni, R.**; Srinivasan, R.; Mii, T.; Bronner, G.
Corporate Source: IBM Microelectronics Semiconductor R and D Center, Hopewell Junction, NY 12533, United States
Conference Title: 2001 International Symposium on VLSI Technology, Systems, and Applications, Proceedings
Conference Location: Hsinchu, Taiwan Conference Date: 20010418-20010420
E.I. Conference No.: 58553
Source: International Symposium on VLSI Technology, Systems, and Applications, Proceedings 2001. p 89-92 (IEEE cat n 01TH8517)
Publication Year: 2001
Language: English
Abstract: A self-aligned buried strap process was developed using a nitride framed self-aligned trench isolation which eliminates parasitic connection between the strap and substrate. The buried strap resistance was lowered and overlayed independently and etch bias was reduced with a selective process. Overlay metrology was improved with a nitride frame process. It was found that trench type DRAM process could be scaled beyond 150 nm ground rule with overlay independent strap formation. (Edited abstract) 5 Refs.

15/3,AB/5 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05804835
E.I. No: EIP00025070084
Title: Slotted vias for dual damascene interconnects in 1Gb DRAMs
Author: Schnabel, R.F.; Bronner, G.; Clevenger, L.; Dobuzinsky, D.; Costrini, G.; Filippi, R.; Gambino, J.; Hug, M.; Iggulden, R.; Lin, C.; Muller, K.P.; Mueller, G.; Nuetzel, J.; **Radens, C.**; Weber, S.; et al
Corporate Source: Siemens Microelectronics, Hopewell Junction, NY, USA
Conference Title: Proceedings of the 1999 Symposium on VLSI Technology
Conference Location: Kyoto, Jpn Conference Date: 19990614-19990616
E.I. Conference No.: 56097
Source: Digest of Technical Papers - Symposium on VLSI Technology 1999. IEEE, Piscataway, NJ, USA. p 43-44
Publication Year: 1999
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: A novel interconnect scheme is presented which has been used to significantly reduce the chip size of an 1Gb SDRAM chip. The key element is the use of slotted vias for low resistance horizontal interconnects. This allows to combine low capacitance/high resistance lines with low resistance/high capacitance lines. The slotted vias are realized by a dual damascene integration scheme without adding an additional mask level or process cost with excellent continuity yield and good electromigration performance. (Author abstract) 3 Refs.

15/3,AB/6 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04970713
E.I. No: EIP98034104383
Title: Thickness and polarity dependence of intrinsic breakdown of ultra-thin reoxidized-nitride for DRAM technology applications
Author: Wu, E.; Hwang, C.; Vollertsen, R.; Shen, H.; Kleinhenz, R.; **Radens, C.**; Strong, A.
Corporate Source: IBM Microelectronics Div, Essex Junction, VT, USA
Conference Title: Proceedings of the 1997 International Electron Devices Meeting
Conference Location: Washington, DC, USA Conference Date: 19971207-19971210
E.I. Conference No.: 48095
Source: Proceedings of the IEEE Hong Kong Electron Devices Meeting 1997. IEEE, Piscataway, NJ, USA,97CH36103. p 77-80
Publication Year: 1997
CODEN: 002525
Language: English
Abstract: This paper discusses the charge-trapping and intrinsic breakdown characteristics of ultra-thin reoxidized nitride with deep-trench capacitor structures for a range of thickness, voltages, and temperatures. Strong polarity dependence of charge-trapping and time-dependent dielectric breakdown (TDDB) is reported. For the first time, a physical model is proposed to relate the asymmetric charge injection and trapping to this intrinsic breakdown characteristic in thin reoxidized nitride. The thickness dependence of TDDB is also investigated and used for a reliability projection of the oxide equivalent thickness down to 2.9 nm. (Author abstract) 8 Refs.

15/3,AB/7 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04862978
E.I. No: EIP97113907001
Title: Novel 1 Gb trench DRAM cell with Raised Shallow Trench Isolation (RSTI)
Author: Alsmeier, I.; Kelleher, K.H.; Beintner, J.; Haensch, W.; **Mandelman, J.A.**; Hoh, P.; Ninomiya, Y.L.; Srinivasan, S.; Bronner, G.
Corporate Source: Siemens Components Inc, Hopewell Junction, NY, USA
Conference Title: Proceedings of the 1997 Symposium on VLSI Technology
Conference Location: Kyoto, Jpn Conference Date: 19970610-19970612
E.I. Conference No.: 47245
Source: Digest of Technical Papers - Symposium on VLSI Technology 1997. IEEE, Piscataway, NJ, USA,97CH36114. p 19-20
Publication Year: 1997
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: The progressive scaling of DRAM cells towards 8F**2 for the 1G generation and beyond requires to design, both channel length and width of the array device in minimum dimensions. Historically the DRAM array device was kept conservatively large to ensure a wide process window for the stringent off current requirement as well as a relaxed doping level to

minimize junction fields and leakage. In this paper, data is presented showing that narrow width effects become dominant in the array transistor design and control of the corner device associated with the shallow trench isolation becomes crucial. A novel Raised Shallow Trench Isolation (RSTI) is proposed as a way of structurally reducing the influences of STI related corner conduction on threshold voltage. This scheme was introduced earlier for the purpose of reducing the size of NAND EEPROM and SRAM cells as well as for a CMOS process. We show its integration into a DRAM cell for the fast time and present data showing the extremely tight control of array threshold voltage achievable with this process. (Author abstract) 6 Refs.

15/3,AB/8 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04565193
E.I. No: EIP96113427059
Title: Floating-body concerns for SOI **dynamic** random access **memory** (DRAM)
Author: **Mandelman, J.A.**; Barth, J.E.; DeBrosse, J.K.; Dennard, R.H. ; Kalter, H.L.; Gautier, J.; Hanafi, H.I.
Corporate Source: IBM Semiconductor Research and Development Cent, Hopewell Junction, NY, USA
Conference Title: Proceedings of the 1996 IEEE International SOI Conference
Conference Location: Sanibel Island, FL, USA Conference Date: 19960930-19961003
E.I. Conference No.: 45625
Source: IEEE International SOI Conference 1996. IEEE, Piscataway, NJ, USA,96CH35937. p 136-137
Publication Year: 1996
CODEN: IISPED
Language: English
Abstract: It has become increasingly difficult to write a usable signal into the **dynamic** random access **memory** (DRAM) storage capacitor because of the nonscalability of threshold voltage which is limited by the subthreshold slope and substrate sensitivity. It is important that the threshold voltage of the DRAM array MOSFET be made as low as possible while meeting the static off-current objective for charge retention. Silicon on insulator (SOI) technology is ideal for these types of applications since its superior subthreshold slope and low substrate sensitivity yield a lower source-follower threshold voltage. However, transient effects of the floating body must be considered for long data retention time and low active power. 4 Refs.

15/3,AB/9 (Item 1 from file: 65)
DIALOG(R)File 65:Inside Conferences

01646271 INSIDE CONFERENCE ITEM ID: CN016784739
Floating-Body Concerns for SOI **Dynamic** Random Access **Memory** (DRAM)
Mandelman, J. A.; Barth, J. E.; DeBrosse, J. K.; Dennard, R. H.
CONFERENCE: International SOI conference-22nd
IEEE INTERNATIONAL SOI CONFERENCE PROCEEDINGS, 1996 P: 136-137
IEEE, 1996
ISSN: 1078-621X ISBN: 0780333160; 0780333152; 0780333179

LANGUAGE: English DOCUMENT TYPE: Conference Papers
CONFERENCE SPONSOR: IEEE Electron Devices Society
CONFERENCE DATE: Oct 1996 (199610) (199610)
NOTE:
Held on Sanibel Island, FL. IEEE cat no 96CH35937 and 96CB35937

15/3,AB/10 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

15657111 PASCAL No.: 02-0363006
Challenges and future directions for the scaling of **dynamic** random-access **memory** (DRAM)

MANDELMAN J A; DENNARD R H; BRONNER G B; DEBROSSE J K; **DIVAKARUNI R**; LI Y; **RADENS C J**
IBM Microelectronics Division East Fishkill Facility, Hopewell Junction, NY 12533, United States

Journal: IBM Journal of Research and Development, 2002, 46 (2-3) 187-212
Language: English

Significant challenges face DRAM scaling toward and beyond the 0.10- mu m generation. Scaling techniques used in earlier generations for the array-access transistor and the storage capacitor are encountering limitations which necessitate major innovation in electrical operating mode, structure, and processing. Although a variety of options exist for advancing the technology, such as low-voltage operation, vertical MOSFETs, and novel capacitor structures, uncertainties exist about which way to proceed. This paper discusses the interrelationships among the DRAM scaling requirements and their possible solutions. The emphasis is on trench-capacitor DRAM technology.

FILE 'REGISTRY'
L1 1 S POLYSILICON/CN

FILE 'HCAPLUS, WPIX, JAPIO'
L2 13 S MOSFET(W)(EDRAM OR ENHANCED(W) RAM OR
ENHANCED(W) DYNAMIC (W) RAM OR
(DYNAMIC)(2N)(RANDOM(W)
ACCESS(W) MEMORY))
L3 3 S (METAL(W) OXIDE(W) SEMICONDUCTOR(2N)
TRANSISTOR)(W)(EDRAM OR ENHANCED(W) RAM OR
ENHANCED(W) DYNAMIC
(W) RAM OR (DYNAMIC)(2N)(RANDOM(W) ACCESS(W) MEMORY))
L4 45 S (MOS OR VMOS OR NMOS OR PMOS)(W)(EDRAM OR
ENHANCED(W) RAM OR ENHANCED(W) DYNAMIC (W) RAM OR
(DYNAMIC)(2N)
(RANDOM(W) ACCESS(W) MEMORY))
L5 45 S (MOS OR VMOS OR NMOS OR PMOS)(W)(EDRAM OR
ENHANCED(W) RAM OR ENHANCED(W) DYNAMIC(W) RAM OR
(DYNAMIC)(2N)(
RANDOM(W) ACCESS(W) MEMORY))
L6 975727 S POLYSILICON OR POLY(W)(SILICON OR SI) OR
SILICON OR HEXSIL OR HGH(W) 600 OR KDB(W) 20 OR
METASILICON OR
SICOMILL(W) 4C OR SICOMILL GRADE 2 OR SILGRAIN(W)
STANDARD OR
SILICON(W) ELEMENT OR SILSO
L7 72 S (MANDELMAN JACK OR MANDELMAN, JACK OR
MANDELMAN, J OR MANDELMAN J)/AU
L8 117 S (DIVAKARUNI, RAMACHANDRA OR DIVAKARUNI
RAMACHANDRA OR DIVAKARUNI, R OR DIVAKARUNI R)/AU
L9 64 S (RADENS, CARL OR RADENS CARL OR RADENS, C
OR RADENS C)/AU
L10 0 S MOSFETEDRAM
L11 4 S MOSFET EDRAM
L12 2 S (MOS OR VMOS OR NMOS OR PMOS MOSFET OR
(METAL(W) OXIDE(W) SEMICONDUCTOR(2N)
TRANSISTOR))(W)(EMBEDDED(W
) DYNAMIC(W) RANDOM(W) ACCESS(W) MEMORY)
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(ENHANCED(W) DYNAMIC(W) RAM) OR
(DYNAMIC)(2N)(RANDOM(W)
ACCESS(W) MEMORY))

FILE 'DPCI'
L14 4 S (US2002094619 OR US6261894)/PN.G,PN.D

```
   FILE 'DPCI'
          SET SMARTSELECT ON
L15         SEL  L14 1- PN :      7 TERMS
          SET SMARTSELECT OFF

   FILE 'HCAPLUS, WPIX, JAPIO'
L16          9 S   L15
L17         61 S   L2 OR L3 OR L4 OR L11 OR L12 OR L13
L18         61 S   L17 NOT L16
L19         25 S   L18 AND L6
L20          5 S   L18 AND GATE(W) CONDUCTOR
L21          4 DUP REMOVE L20 (1 DUPLICATE REMOVED)
L22          3 S   L18 AND GUARD(W) RING
L23     132038 S   MOSFET OR METAL(W) OXIDE(W) SEMICONDUCTOR(2
               N) TRANSISTOR OR MOS OR VMOS OR NMOS OR PMOS
L24      31136 S   EDRAM OR ENHANCED(W) RAM OR ENHANCED(W)
               DYNAMIC(W) RAM OR (DYNAMIC)(2N)(RANDOM(W) ACCESS(W)
MEMORY OR
               (EMBEDDED(W) DYNAMIC(W) RANDOM(W) ACCESS(W) MEMORY))
OR DRAM
L25       3195 S   L23 AND L24
L26         25 S   L19 OR L22 NOT L20
L27         24 DUP REMOVE L26 (1 DUPLICATE REMOVED)
L28         36 S   L18 NOT (L19 OR L20 OR L22 OR L16)
L29         35 DUP REMOVE L28 (1 DUPLICATE REMOVED)
L30       3128 S   L25 NOT (L17 OR L16)
L31       1246 S   L30 AND (L6 OR L1)
L32         21 S   L31 AND GATE(W) CONDUCTOR
L33          1 S   L31 AND GUARD(W) RING
L34        120 S   L31 AND (WORD(W) LINE OR WORDLINE)
L35          6 S   L34 AND INTERCONNECT?
L36         29 S   L34 AND ARRAY
L37         83 S   L34 AND (BIT(W) LINE OR BITLINE)
L38         22 S   L32 OR L33
L39         21 DUP REMOVE L38 (1 DUPLICATE REMOVED)
L40          6 S   L35 NOT L38
L41          6 DUP REMOVE L40 (0 DUPLICATES REMOVED)
L42         24 S   L36 NOT (L38 OR L40)
L43          0 S   JP11286865/AP,PRN

   FILE 'WPIX, JAPIO, INPADOC'
L44          5 S   JP1999-286865/AP,PRN

   FILE 'HCAPLUS, WPIX, JAPIO'
L45         72 S   (MANDELMAN JACK OR MANDELMAN, JACK OR
               MANDELMAN, J OR MANDELMAN J)/AU
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L46	117 S	(DIVAKARUNI, RAMACHANDRA OR DIVAKARUNI RAMACHANDRA OR DIVAKARUNI, R OR DIVAKARUNI R)/AU
L47	64 S	(RADENS, CARL OR RADENS CARL OR RADENS, C OR RADENS C)/AU
L48	221 S	(L45 OR L46 OR L47)
L49	6 S	L48 AND L17
L50	58 S	L48 AND L23
L51	38 S	L50 AND L24
L52	23 S	L51 AND GATE(W) CONDUCTOR
L53	25 S	L51 AND (L6 OR L1)
L54	118 S	L16 OR L17 OR L26 OR L36 OR L32
L55	34 S	L52 OR L53
L56	18 S	L55 NOT L54

```
     FILE 'WPIX, JAPIO' ENTERED AT 09:45:35 ON 09 AUG 2002
L1       161048 S (METAL()OXIDE()SEMICONDUCTOR) OR VMOS OR MOS OR NMOS OR PMOS
L2         4251 S (U21-C01B3 OR U23-J01A5C)/MC
L3        10003 S (H03K-019/094? OR H03B-021 OR H03D-007)/IC
L4        11337 S ERAM OR CDRAM OR ENHANCED()DRAM OR ENHANCEDDRAM OR DYNAMIC(2N
L5         4838 S ENHANCED()DYNAMIC()RANDOM()ACCESS()MEMORY OR EDRAM OR CDRAM O
L6        26079 S DRAM OR D()RAM OR DYNAMIC()RAM OR DYNAMICRAM OR (D OR DYNAMIC
L7       344165 S EMBED#### OR IMBED#### OR ENTRENCH? OR FASTEN? OR INFIX## OR
L8       250209 S VERTICUL? OR PERPENDICULAR OR UPRIGHT
L9         4466 S (L1-3)AND(L4-6)
L10      347567 S POLYSILICON OR  SILICON OR HEXSIL OR HGH()600 OR KDB()20OR ME
L11         860 S L9 AND L10
L12         659 S L11 AND GATE
L13          26 S L12 AND L7
L14           2 S L12 AND L8
L15           2 S L14 NOT L13
L16          11 S L12 AND HIGH()PERFORMANCE
L17           0 S L14 NOT (L13 OR L15)
L18           8 S L16 NOT (L13 OR L15)
L19         147 S L12 AND (DUAL OR DOUBLE OR TWO OR PAIR)
L20          29 S L19 AND (WORDLINE OR WORD()LINE)
L21          25 S L20 NOT (L13 OR L15 OR L16)
L22          33 S L19 AND (BITLINE OR BIT()LINE)
L23          13 S L22 NOT (L13 OR L15 OR L16 OR L20)
L24         950 S (L1-3)(3N)(L4-6)
L25         142 S L24 AND (BITLINE OR BIT()LINE)
L26          72 S L25 AND (WORDLINE OR WORD()LINE)
L27           3 S L26 AND L7
L28           0 S L27 NOT (L13 OR L15 OR L16 OR L20 OR L22)
L29          66 S L26 NOT (L13 OR L15 OR L16 OR L20 OR L22)
L30           1 S L29 AND IMPLANT?
L31           8 S L29 AND L10
L32         485 S (L1-3)(2N)(L4-5)
L33          75 S L32 AND (WORDLINE OR WORD()LINE)
L34          42 S L33 AND (BITLINE OR BIT()LINE)
L35           0 S L34 NOT (L13 OR L15 OR L16 OR L20 OR L22 OR L26 OR L30 OR L3
L36         103 S L32 AND L10
L37           8 S L36 AND L7
L38           1 S L37 NOT (L13 OR L15 OR L16 OR L20 OR L22 OR L26 OR L30 OR L3
L39           1 S L36 AND L8
L40           0 S L39 NOT (L13 OR L15 OR L16 OR L20 OR L22 OR L26 OR L30 OR L3
L41        3920 S L4(2N)L6
L42          78 S L41(2N)(L1-3)
L43          70 S L42 NOT (L13 OR L15 OR L16 OR L20 OR L22 OR L26 OR L30 OR L3
L44          17 S L43 AND L10
L45         542 S (L1-3)(3N)(L4-5)
L46         242 S L45 AND L6
L47          67 S L46 AND L10
L48          10 S L47 AND (WORDLINE OR WORD()LINE)
L49           2 S L48 NOT (L13 OR L15 OR L16 OR L20 OR L22 OR L26 OR L30 OR L3
L50       11343 S (EDRAM OR CDRAM OR ENHANCED()DRAM OR ENHANCEDDRAM OR DYNAMIC(
L51          45 S EDRAM OR CDRAM OR ENHANCED()DRAM OR ENHANCEDDRAM
L52          44 S L51 NOT (L13 OR L15 OR L16 OR L20 OR L22 OR L26 OR L30 OR L3
L53         170 S EDRAM OR CDRAM OR EMBEDDED()DRAM OR EMBEDDEDDRAM
L54          69 S (ENHANCED OR EMEBBED)()DYNAMIC()RANDOM()ACCESS()MEMORY OR((CA
L55         232 S L53 OR L54
L56          18 S L55 AND (L1-3)
L57          12 S L56 NOT (L13 OR L15 OR L16 OR L20 OR L22 OR L26 OR L30 OR L3
```

L58	1756	S (L1-3) AND (L50 OR L51 OR L53 OR L54)
L59	1637	S L58 NOT (L13 OR L15 OR L16 OR L20 OR L22 OR L26 OR L30 OR L3
L60	867	S L59 AND L6
L61	176	S L60 AND L10
L62	9	S L61 AND (WORDLINE OR WORD()LINE)AND (BITLINE OR BIT()LINE)

L13 ANSWER 1 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 2002-458612 [49] WPIX
DNN N2002-361733 DNC C2002-130905
TI Semiconductor **memory**, **e**.g. **dynamic** **random** access **memory**, has storage **MOS** transistor, diode and transfer **MOS** transistor which are **embedded** in trench formed on a **silicon** substrate.
DC L03 U11 U13
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 2002110818 A 20020412 (200249)* 13p
ADT JP 2002110818 A JP 2000-296080 20000928
PRAI JP 2000-296080 20000928
AB JP2002110818 A UPAB: 20020802
NOVELTY - A diode is electrically connected to a **gate** electrode and the drain area of a storage **MOS** transistor, respectively. The **gate** electrode and drain area of a transfer **MOS** transistor are connected to the word line and bit line, respectively. Each memory cell includes the storage **MOS** transistor, transfer **MOS** transistor and the diode which are **embedded** in a trench (11) formed on a **silicon** substrate (10).
DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for semiconductor memory manufacturing method.
USE - Semiconductor **memory e**.g. **dynamic** **random** access **memory** (**DRAM**).
ADVANTAGE - Since the storage **MOS** transistor, the transfer **MOS** transistor and the diode of the memory cell are **embedded** in the trench, the memory cell occupancy area is reduced and therefore the manufacturing process is simplified.
DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of the memory cell.
Silicon substrate 10
Trench 11
Dwg.3/19

L13 ANSWER 2 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 2002-314598 [35] WPIX
DNN N2002-246264 DNC C2002-091394
TI Fabrication of **embedded dynamic random** access **memory** with salicide logic cells and memory cells involves forming **silicon** nitride layer on substrate and **gate** structures on logic cell and memory cell regions.
DC L03 U11 U13
IN LIEN, W Y
PA (WORL-N) WORLDWIDE SEMICONDUCTOR MFG CORP
CYC 1
PI US 6338993 B1 20020115 (200235)* 8p
ADT US 6338993 B1 US 1999-376481 19990818
PRAI US 1999-376481 19990818
AB US 6338993 B UPAB: 20020603
NOVELTY - Fabricating an **embedded dynamic** **random** access **memory** with salicide logic cells and memory cells comprises: forming **silicon** nitride layer on substrate and on **gate** structures on logic cell region and memory cell region; and forming salicide layer on source/drain regions of logic cell region. The **gate** structure of memory cell region is protected by **silicon** nitride layer.
DETAILED DESCRIPTION - Fabricating an **embedded**

dynamic random access **memory (DRAM)** with salicide logic cells and memory cells involves providing a substrate (200) having isolation regions formed to define a p-type **metal oxide semiconductor** (PMOS) region (10), an n-type **metal oxide semiconductor (NMOS)** region (20) and a memory cell region (30). A first **gate** structure (231) is formed on the PMOS region. A second **gate** structure (232) is formed on the **NMOS** region. A third **gate** structure is formed on the memory cell region. Light-doped-drain (LDD) regions (300) are formed in the substrate adjacent the **gate** structures. A conformal **silicon** nitride layer (400) is formed on the substrate and the **gate** structures. A first photoresist pattern is formed to cover the PMOS region and the memory cell region and to expose the **NMOS** region. The **silicon** nitride layer is etched to form second nitride spacers of the second **gate** structure after the first photoresist pattern is formed. An N-type conductive ion implantation process is performed to form N-type source/drain regions (320) of an **NMOS** device on the **NMOS** region and dope N-type conductive ions into the second **gate** structure. The first photoresist pattern is stripped. A second photoresist pattern is formed to cover the **NMOS** region and the memory cell and to expose the PMOS region. The **silicon** nitride layer is etched to form first nitride spacers of the first **gate** structure after the second photoresist pattern is formed. A P-type conductive ion implantation process is performed to form P-type source/drain regions (310) of a PMOS device on the PMOS region and dope P-type conductive ions into the first **gate** structure. The second photoresist pattern is stripped. Finally, a salicide process is performed to form a salicide layer (500) on the P-type source/drain regions, first **gate** structure, N-type source/drain regions, and second **gate** structure. The third **gate** structure is protected by the **silicon** nitride layer during the salicide process.

USE - The method is used for fabricating an **embedded DRAM** with salicide logic cells and memory cells.

ADVANTAGE - The method forms salicide on the peripheral logic region of the **embedded DRAM** without using a salicide block mask layer to protect the memory cell region of the **embedded DRAM** and without oxide wet dip to prevent oxide loss in the field oxide.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-section view of a substrate.

PMOS region 10
NMOS region 20
Memory cell region 30
Substrate 200
Gate oxide layer 220
Doped **polysilicon** layer 240
Polycide layer 250
Cap layer 260
First **gate** structure 231
Second **gate** structure 232
LDD regions 300
P-type source/drain regions 310
N-type source/drain regions 320
Silicon nitride layer 400
Salicide layer 500
Plug 700
Dwg.7/7

L13 ANSWER 3 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 2002-225220 [28] WPIX
DNN N2002-172644 DNC C2002-068650
TI Manufacture of semiconductor device involves forming thin thermally-oxidized **polysilicon** side-wall film that blocks oxidation of refractory metal nitride barrier layer.
DC L03 U11
IN CUNNINGHAM, J A
PA (PHIG) PHILIPS SEMICONDUCTORS INC
CYC 1
PI US 2001013600 A1 20010816 (200228)* 10p
ADT US 2001013600 A1 Div ex US 1998-136482 19980819, US 2001-783689 20010214
FDT US 2001013600 A1 Div ex US 6208004
PRAI US 1998-136482 19980819; US 2001-783689 20010214
AB US2001013600 A UPAB: 20020502
NOVELTY - A semiconductor device is made by forming a thin thermally-oxidized **polysilicon** side-wall film (114a, 114b) against underlying doped **polysilicon** layer, metal nitride barrier layer (108), overlying silicide layer, and cap dielectric. The sidewall film is arranged to block oxidation of the thin refractory metal nitride barrier layer.

DETAILED DESCRIPTION - Manufacture of semiconductor device having a polycide transistor **gate** electrode involves:

(a) forming a thin refractory metal nitride barrier layer between doped **polysilicon** layer and overlying silicide layer to reduce diffusion transport of dopants between them; and

(b) forming a thin thermally-oxidized **polysilicon** side-wall film against the underlying doped **polysilicon** layer, the metal nitride barrier layer, the overlying silicide layer, and the cap dielectric. The sidewall film is arranged to block oxidation of the thin refractory metal nitride barrier layer.

USE - For forming complementary **metal oxide semiconductors** for high-performance logic applications such as microprocessors or **embedded dynamic random access memory** implementations.

ADVANTAGE - The method provides improved **gate** electrode exhibiting greater tolerances to higher temperature annealing treatments. It avoids threshold voltage shifts and possible poly-depletion problems caused by rapid diffusion of dopants. It also prevents silicide agglomeration which in turn prevents resistivity increase. It further solves the problem of increased junction leakage of the prior art.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a semiconductor **gate** structure.

Refractory metal nitride barrier layer 108
Sidewall film 114a, 114b
Dwg.1/4

L13 ANSWER 4 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 2002-214352 [27] WPIX
DNN N2002-163982 DNC C2002-065555
TI Formation of **metal oxide semiconductor** field effect transistor/**embedded dynamic random access memory** array by forming bitlines and local interconnects by salicidation, and hard masks defining bitline and support **gate** region.
DC L03 U11 U12 U13 U14
IN DIVAKARUNI, R; MANDELMAN, J A; RADENS, C J
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1

PI US 6261894 B1 20010717 (200227)* 23p
ADT US 6261894 B1 US 2000-706492 20001103
PRAI US 2000-706492 20001103
AB US 6261894 B UPAB: 20020429

NOVELTY - A **metal oxide semiconductor** field effect transistor/**embedded dynamic random** access **memory** array is made by forming and patterning doped glass material to form hard masks that define bitline of a memory structure and support **gate** region; forming **gate** conductor guard ring around the array region; and forming bitlines and local interconnects by salicidation of **polysilicon**.

DETAILED DESCRIPTION - Formation of a dual work function high performance **metal oxide semiconductor** field effect transistor (MOSFET)/**embedded dynamic random** access **memory** array (**EDRAM**) involves (a) providing a memory structure with array region(s) having **dynamic random** access **memory** (**DRAM**) cells **embedded** in a substrate (the **DRAM** cells being connected by bitline diffusion region capped with oxide layer), and support region(s) separated from the array region by an isolation region; (b) forming a patterned nitride layer on all exposed surfaces in the array region(s) and on a portion of the isolation region; (c) forming a **gate** oxide on the substrate in the support region; (d) forming a stack comprising **polysilicon** layer and dielectric capping layer on all exposed surfaces of the memory structure; (e) removing the dielectric capping layer, **polysilicon** layer and nitride layer from the array region(s); (f) forming wordlines over the **DRAM** cells; (g) forming spacers on exposed sidewalls of the wordlines in the array region(s) as well as on the exposed sidewalls of the stack remaining in the structure; (h) forming a block mask over the support region(s) and over at least a portion of one of the **DRAM** cells that is adjacent to the isolation region (the block mask does not cover the oxide capping layer); (i) removing the oxide capping layer over the bitline diffusion regions and stripping the block mask; (j) forming a patterned second **polysilicon** layer over the array region(s) and the stack present on the isolation region, and removing the dielectric capping layer in the support region(s); (k) forming a doped glass material layer (64) over all surfaces in the array region(s) and the support region(s); (l) patterning the doped glass material layer to form hard masks that define bitline of the memory structure in the array region(s) and hard masks that define support **gate** region in the support region(s); (m) removing exposed second **polysilicon** layer from the array region(s) and the isolation region, while simultaneously removing exposed portions of the first **polysilicon** layer in the support region(s), by which a **gate** conductor guard ring is formed on the isolation region and the support **gate** region is formed on the support region(s); (n) removing the hard masks from the array region(s) and from the support region(s) and forming a screen oxide layer on any exposed **silicon** surfaces; (o) forming source and drain regions about the support **gate** region; and (p) removing oxide overlying the bitline, support **gate** region, and source and drain regions to expose **silicon** surfaces and saliciding the exposed **silicon** surfaces to provide salicide regions over the bitline, the **gate** region and source and drain regions.

USE - For fabricating dual work function high-performance support MOSFETs/**EDRAM** arrays.

ADVANTAGE - The method saves two deep-UV masks relative to conventional processing. It decouples the support and arraying processing steps. It provides salicided **gates**, source/drain regions and

bitlines. It provides, in some instances, local interconnects at no additional processing costs.

DESCRIPTION OF DRAWING(S) - The figure shows the initial memory structure after the doped glass layer is patterned to form a hard mask.

Doped glass material layer 64

Dwg.8/27

L13 ANSWER 5 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 2001-450371 [48] WPIX
DNN N2001-333330 DNC C2001-135968
TI Formation of **dynamic random** access **memory** array and support **metal oxide semiconductor** field effect transistors involves saliciding tops of bitline diffusion stud landing pad in array and **gate** conductors for support transistors.
DC L03 U11
IN DIVAKARUNI, R; GRUENING, U; MANDELMAN, J A; RUPP, T S; MANDELMAN, J; RUPP, T
PA (IBMC) INT BUSINESS MACHINES CORP; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP
CYC 23
PI US 6258659 B1 20010710 (200148)* 12p
WO 2002045130 A2 20020606 (200238) EN
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: CN JP KR
ADT US 6258659 B1 US 2000-725412 20001129; WO 2002045130 A2 WO 2001-US44625 20011128
PRAI US 2000-725412 20001129
AB US 6258659 B UPAB: 20010829

NOVELTY - Formation of memory array and support transistors comprises applying a block mask to protect supports while stripping nitride layer from array and etching exposed **polysilicon** layer to the top of **gate** oxide layer and to form bitline diffusion stud landing pad in array and **gate** conductors for the support transistors; and saliciding the tops of the landing pad and the **gate** conductors.

DETAILED DESCRIPTION - Formation of memory array and support transistors comprises forming a trench capacitor in a **silicon** substrate (11) having a **gate** oxide layer (18), **polysilicon** layer, and top dielectric nitride layer. A patterned mask is applied over the array and support areas. Recesses are formed in the nitride layer, **polysilicon** layer and shallow trench isolation region (14). A silicide and an oxide cap are formed in the recesses in the nitride layer, **polysilicon** layer and shallow trench isolation region. A block mask is applied to protect the supports while stripping the nitride layer from the array. The exposed **polysilicon** layer is etched to the top of the **gate** oxide layer. The nitride layer is stripped from the support region and a **polysilicon** layer is deposited over the array and support areas. A mask is applied to pattern and forms a bitline diffusion stud landing pad in the array and **gate** conductors (28) for the support transistors. The tops of the landing pad and the **gate** conductors are salicided. An interlevel oxide layer (36) is applied and then vias in the interlevel oxide layer are opened for establishing conductive wiring channels.

USE - For forming **dynamic random** access **memory** (**DRAM**) array and support **metal oxide semiconductor** field effect transistors (MOSFETs).

ADVANTAGE - The method fabricates very high-density **embedded DRAM** and very high-performance support MOSFETs. It provides for a

bitline contact self-aligned to the active area, eliminates boron-phosphosilicate glass reflow step, reduces thermal budget, and allows shallower source/drains.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a **DRAM** array and support MOSFET at a production stage.

Silicon substrate 11
Shallow trench isolation region 14
Gate oxide layer 18
Gate conductors 28
Interlevel oxide layer 36

Dwg.18/18

L13 ANSWER 6 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 2000-664318 [64] WPIX
DNN N2000-492275 DNC C2000-201224
TI Fabrication of **embedded dynamic random** access **memory** by forming insulating layer and self-aligned silicide layer.
DC L03 U11 U12 U13
IN CHEN, J; CHEN, T; LIN, Y
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 6133130 A 20001017 (200064)* 13p
ADT US 6133130 A US 1998-181530 19981028
PRAI US 1998-181530 19981028
AB US 6133130 A UPAB: 20001209

NOVELTY - An **embedded dynamic random** access **memory** (**DRAM**) is fabricated by forming an insulating layer on an interchangeable source/drain regions of second **MOS** transistor, and forming self-aligned silicide layer.

DETAILED DESCRIPTION - Fabrication of an **embedded DRAM** includes a self-aligned silicide technology. The **embedded DRAM** is fabricated on a **silicon** substrate (200) having first **metal-oxide semiconductor** (**MOS**) transistor in a logic device region (203) and second **MOS** transistor in a memory device region (205) separated by an isolation structure (201). Each of the **MOS** transistors has a **gate** including **polysilicon** and an interchangeable source/drain region (229) on each side of the **gate** in the substrate. An insulating layer (212b) is formed on the interchangeable source/drain region of the second **MOS** transistor. A self-aligned silicide (salicide) layer (224) is formed over the exposed substrate at least on the exposed **gates** of first and second **MOS** transistors and interchangeable source/drain regions of the first **MOS** transistor.

USE - For fabricating an **embedded DRAM**.

ADVANTAGE - The invention simultaneously forms the self-aligned layer on the first and second **gate** structures to increase the conductivity of the **gate** structures, thus simplifying the fabrication process. The inter-layer diffusion at the interface is avoided because the salicide layer is formed after the interchangeable source/drain region is formed. An agglomeration of the salicide layer due to thermal budget also does not occur since it is formed after rapid thermal anneal process.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of a fabrication process of an **embedded DRAM**

Substrate 200
Isolation structure 201
Logic device region 203

Memory device region 205
Insulating layer 212b
Salicide layer 224
Interchangeable source/drain region 229
Dwg.2H/2

L13 ANSWER 7 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 2000-413328 [36] WPIX
CR 2001-595222 [48]
DNN N2000-406712
TI Single **polysilicon** **DRAM** memory cell comprises data storing transistor whose threshold voltage is modulated by selectively biasing p-well to predetermined voltage, to store data.
DC U12 U13 U14
IN CHI, M
PA (SHID-N) SHIDA INTEGRATED CIRCUIT CO LTD; (WORL-N) WORLDWIDE SEMICONDUCTOR MFG CORP
CYC 2
PI CN 1250949 A 20000419 (200036)*
US 6087690 A 20000711 (200051)B 7p
ADT CN 1250949 A CN 1998-122620 19981123; US 6087690 A US 1998-170863 19981013
PRAI US 1998-170863 19981013
AB US 6087690 A UPAB: 20001016 ABEQ treated as Basic
NOVELTY - The **DRAM** cell comprises an n-**MOS** transistor formed by an n+ region (113), a p-well (105), a deep n-well (103), a **gate** (107) and a conductive reset p+ junction (124). The p-well stores the body bias voltage which modulates the threshold voltage of the n-**MOS** transistor. The data is stored in a transistor by selectively biasing the p-well to a predetermined voltage.

DETAILED DESCRIPTION - The n-**MOS** transistor in the **DRAM** comprises a p-well inside the deep n-well. The **gate** is formed on the surface of an n-well with a p-well terminates under the **gate** structure. The n+ region is formed in the p-well adjacent to the side walls of the **gate** structure. The conductive reset p+ region is attached to the p-well through a transistor switch.

USE - **DRAM** cell can be used in **embedded** logic applications.

ADVANTAGE - The read operation is non-destructive, as the charge in the p-well is not consumed by the read operation. The state of memory is determined by measuring the amount of current flow. The **DRAM** cell is compatible with the logic, as memory and logic circuit are placed on single chip.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic form complex **DRAM** cell.
Deep n-well 103
p-well 105
Gate 107
n+ region 113
p+ junction 124
Dwg.5/7
AB CN 1250949 A UPAB: 20011121
NOVELTY - The **DRAM** cell comprises an n-**MOS** transistor formed by an n+ region (113), a p-well (105), a deep n-well (103), a **gate** (107) and a conductive reset p+ junction (124). The p-well stores the body bias voltage which modulates the threshold voltage of the n-**MOS** transistor. The data is stored in a transistor by selectively biasing the p-well to a predetermined voltage.

DETAILED DESCRIPTION - The n-**MOS** transistor in the **DRAM** comprises a p-well inside the deep n-well. The **gate**

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DESCRIPTION OF DRAWING(S) - The figure shows a schematic form complex **DRAM** cell.

Deep n-well 103
p-well 105
Gate 107
n+ region 113
p+ junction 124
Dwg.5/7

L13 ANSWER 8 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 2000-191806 [17] WPIX
DNN N2000-142941
TI Semiconductor memory such as **DRAM** has active region formed in memory cell area in preset shape to concentrate electric field during bias voltage application to **gate** electrode.
DC U11 U13
PA (MATE) MATSUSHITA ELECTRONICS CORP
CYC 1
PI JP 2000036544 A 20000202 (200017)* 23p
ADT JP 2000036544 A JP 1998-204914 19980721
PRAI JP 1998-204914 19980721
AB JP2000036544 A UPAB: 20000405

NOVELTY - A groove (106) for element separation is formed at both sides of **MOS** transistor. An implanting insulating film (108) is **embedded** on the groove. An active region of the **MOS** transistor, consisting of channel, source and drain areas formed opposite to opening end of groove has a preset shape to concentrate electric field during application of bias voltage to the **gate** electrode of the **MOS** transistor. DETAILED DESCRIPTION - The memory has a memory cell array area (105) surrounded by a peripheral circuit areas (112,113). Each memory cell has a source area and a drain area formed on the surface of a P type **silicon** substrate (101). A **MOS** transistor with a **gate** electrode is formed through a **gate** insulating film on a channel area arranged between the source and drain area. The groove is formed at both sides of **MOS** transistor along channel width direction on a P type **silicon** substrate. An INDEPENDENT CLAIM is also included for semiconductor memory manufacturing method.

USE - For **e**.g. **DRAM**.

ADVANTAGE - Enables to store two different types of information in memory cell area by forming two **MOS** transistors with two different threshold voltage levels on active region. Enables to expand memory cell area. DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of semiconductor memory, top view of memory cell array area and circuit diagram of memory cell area. (101) P type **silicon** substrate; (105) Memory cell area; (106) Groove; (108) **Silicon** oxide film; (112,113) Peripheral circuit areas.
Dwg.1/20

L13 ANSWER 9 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1999-239329 [20] WPIX
DNN N1999-178595
TI Depleted lean channel transistor semiconductor device e.g. **MOS** transistor - has pillar shaped protrusion on substrate forming **gate** electrode with insulation film on sides for electrically isolating it from substrate.
DC U11 U12
IN IWASA, S; KAWAMATA, T
PA (YAWA) NIPPON STEEL CORP
CYC 2
PI JP 11068069 A 19990309 (199920)* 47p
US 6288431 B1 20010911 (200154)
ADT JP 11068069 A JP 1998-110237 19980406; US 6288431 B1 US 1998-54399 19980403
PRAI JP 1997-173112 19970613; JP 1997-102743 19970404
AB JP 11068069 A UPAB: 19990525
NOVELTY - A pillar shaped protrusion (11) is formed a `P' type **silicon** substrate (1) with four center portions covered by a **gate** electrode (21). A pair of impurity diffusion layer (22) is formed on pillar shaped protrusion and on both sides of **gate** electrode. An insulating film (23) formed on a substrate (1) is **embedded** on sides of pillar shaped protrusions. DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for semiconductor device manufacturing method.

USE - For **DRAM**, EEPROM.

ADVANTAGE - A semiconductor device which has high drive capability and hyper fine structure is materialized. DESCRIPTION OF DRAWING(S) - The figure shows schematic perspective diagram of structure of the **MOS** transistor. (1) Substrate; (11) Pillar shaped protrusion; (21) **Gate** electrode; (22) Impurity diffusion layer; (23) Insulating film.
Dwg.1/45

L13 ANSWER 10 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1998-247451 [22] WPIX
DNN N1998-196141
TI Conductor pattern arrangement for VLSI e.g. for memory IC such as **D-RAM**, **MOS**-RAM - has electrically conductive thin film formed at bottom of side attachment wall spacer equipped with groove formed by etching.
DC U11 U13 U14
PA (HAIL-I) HAI L
CYC 1
PI JP 10079482 A 19980324 (199822)* 358p
ADT JP 10079482 A JP 1996-242502 19960809
PRAI JP 1996-242502 19960809
AB JP 10079482 A UPAB: 19980604
The arrangement includes an electrically conductive thin film formed surrounding the side attachment wall of several semiconductor devices. The electrically conductive film is formed at the bottom of a side attachment wall spacer equipped with a groove formed by etching.

A memory cell equipped with an **embedded** bit line and an **embedded gate** transistor is provided. Each transistor having the same **gate** and channel lengths are integrated in a single chip. The bit line consists of a metallic material, **polysilicon** or polycide material. The word line consists of **polysilicon** and metallic materials.

ADVANTAGE - Improves high densification and operation performance of memory IC.
Dwg.0/179

L13 ANSWER 11 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1997-124895 [12] WPIX
DNN N1997-103145 DNC C1997-040079
TI Semiconductor memory mfg method **e**.g. for **DRAM** - involves performing anisotrophy etching and side attachment wall pattern formation repeatedly for **silicon** oxide films and polycrystalline films which act as electrode plates of capacitor.
DC L03 U11 U13 U14
PA (YAWA) NIPPON STEEL CORP
CYC 1
PI JP 09008249 A 19970110 (199712)* 9p
ADT JP 09008249 A JP 1995-176632 19950620
PRAI JP 1995-176632 19950620
AB JP 09008249 A UPAB: 19970320
The method involves forming a **MOS** transistor with a **gate** electrode (23) and a pair of impurity diffusion layer on a substrate (21). An insulating film (27) is formed over the **MOS** transistor. A contact hole is **embedded** in a first polycrystalline **silicon** film (32) to one side of the impurity diffusion layer. A **silicon** nitriding film (30) and a first **silicon** oxide film (31) are formed orderly which are then selectively eliminated to expose upper area of the impurity diffusion layer. Then, a second polycrystalline **silicon** film (34) and a second **silicon** oxide film (33) are formed with a spacer (35) along side walls of holes. A third polycrystalline **silicon** film (36) and a third **silicon** film are formed over the whole surface and are selectively etched until the third polycrystalline film is exposed.

A side attachment wall pattern of third **silicon** oxide film is then formed. The third polycrystalline **silicon** film is etched until second **silicon** oxide film to form side attachment wall pattern of third polycrystalline **silicon** film. The processes of etching and side wall pattern formation is continued so that the side wall pattern of the second **silicon** film, the second polycrystalline **silicon** film are formed. Then, a fourth polycrystalline **silicon** film (38) is formed over the entire surface which is etched and a side attachment wall pattern of fourth polycrystalline **silicon** film is formed. The side attachment wall pattern of the first, second and third **silicon** oxide films are then eliminated. A capacitor dielectric film (37) is formed on the surface of a storage electrode consisting of second, third and fourth polycrystalline films. A plate electrode which consists of a fifth polycrystalline **silicon** film is formed on the capacitor dielectric film.

ADVANTAGE - Increases accumulative electric charge. Forms high integration of **DRAM**, reliably. Enlarges surface area of storage electrode per unit planar product.
Dwg.1/12

L13 ANSWER 12 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1994-295441 [37] WPIX
DNN N1994-232496
TI **DRAM** structure using trench-**embedded** transistor-capacitor arrangement - has MOST buried in **gate**, capacitor formed by length of **gate** and surface of substrate, and wire line formed from phosphorus-doped poly **silicon**.
DC U13 U14

IN YAMADA, T
PA (TOKE) TOSHIBA KK
CYC 4
PI DE 4408764 A1 19940922 (199437)* 43p
JP 06268174 A 19940922 (199443) 21p
US 5502320 A 19960326 (199618) 42p
DE 4447730 A1 19970821 (199739) 1p
DE 4408764 C2 19980430 (199821) 34p
KR 161357 B1 19981201 (200032)
ADT DE 4408764 A1 DE 1994-4408764 19940315; JP 06268174 A JP 1993-80116 19930315; US 5502320 A US 1994-212796 19940315; DE 4447730 A1 Div ex DE 1994-4408764 19940315, DE 1994-4447730 19940315; DE 4408764 C2 DE 1994-4408764 19940315; KR 161357 B1 KR 1994-4967 19940314
FDT DE 4447730 A1 Div ex DE 4408764; DE 4408764 C2 Div in DE 4447730
PRAI JP 1993-80116 19930315
AB DE 4408764 A UPAB: 19941216

DRAM cells are realised by a **MOS** transistor and capacitor. The **MOS** transistor is buried in the **gate** structure, and the capacitor is formed by the length of the **gate** structure and the surface of the substrate. An isolation trench (3) is made in the direction of word lines, and an oxide insulator is formed.

A word line (7) is formed in a linear trench, followed by a **gate** insulation layer (6) of SiO_2. Then in the **gate** -trench, a word line (7) and electrode are formed from phosphorus-doped **polysilicon**.

ADVANTAGE - High circuit density possible, good tolerance towards mfg. process masking variation, low leakage.
Dwg.2b/35

L13 ANSWER 13 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1992-309418 [38] WPIX
DNN N1992-236864
TI **DRAM** integrated circuit with floating electrode capacitor memory cell - has pair of **MOS** transistors formed on substrate and stack capacitor in trench between transistors and defined by word lines which serve as transistor **gates** with capacitor layers extending partly over word lines.
DC U11 U13 U14
IN ADAN, A O
PA (SHAF) SHARP KK
CYC 7
PI EP 503199 A2 19920916 (199238)* EN 14p
R: DE GB IT NL
JP 04283963 A 19921008 (199247) 7p
EP 503199 A3 19921104 (199342)
US 5606189 A 19970225 (199714) 14p
EP 503199 B1 19970409 (199719) EN 16p
R: DE GB IT NL
DE 69125593 E 19970515 (199725)
KR 251217 B1 20000415 (200124)
ADT EP 503199 A2 EP 1991-311823 19911219; JP 04283963 A JP 1991-48142 19910313; EP 503199 A3 EP 1991-311823 19911219; US 5606189 A Cont of US 1991-786831 19911101, US 1993-111967 19930826; EP 503199 B1 EP 1991-311823 19911219; DE 69125593 E DE 1991-625593 19911219, EP 1991-311823 19911219; KR 251217 B1 KR 1992-3966 19920311
FDT DE 69125593 E Based on EP 503199
PRAI JP 1991-48142 19910313
AB EP 503199 A UPAB: 19931202

The **dynamic RAM memory** comprises a pair of N

mos transistors formed side by side on a p-type substrate (1). A trench is formed between adjacent impurity regions (A,B), each at one end of transistors. A stack capacitor, formed in the trench between the adjacent active regions. A first electrode layer (4) of **polysilicon** connected to one active region (A), a capacitor insulating layer (5), and second **polysilicon** electrode layer (6) connected to the second transistor impurity region (B), through a contact strap (8).

The layers are formed one over another and are, **embedded** in trench. Pref. the stack capacitor extends to partly cover a word line (WL) serving as the **gate** of each **mos** transistor. In production the trench is self registered between the work lines without misalignment.

USE/ADVANTAGE - Increase capacitance with improved reproducibility for three-element, two-bit storage cell. Small area. Increased integration density. Simple mfg. process. 50 per cent cell utility factor.
17/23

L13 ANSWER 14 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1987-243505 [35] WPIX
DNN N1987-182127 DNC C1987-102868
TI Dynamic **MOS** random access memory - has trench type capacitor electrodes acting as nodes for memory cells.
DC L03 U11 U13 U14
IN WADA, M
PA (TOKE) TOSHIBA KK
CYC 2
PI DE 3640363 A 19870827 (198735)* 12p
JP 62193273 A 19870825 (198739)
DE 3640363 C 19920213 (199207)
ADT DE 3640363 A DE 1986-3640363 19861126; JP 62193273 A JP 1986-35467 19860220
PRAI JP 1986-35467 19860220
AB DE 3640363 A UPAB: 19930922
A **dynamic MOS** random **memory** has a substrate with a separate capacitor electrode which is inserted in insulation in a trench. A vapour-deposited insular semiconductor layer, joined to the capacitor electrode carrier source and drain zones, also a **gate** insulating layer with a **gate** electrode.

A p-type **silicon** substrate (1) has several trenches (2), lined with thermally produced oxide layers (3) for the n(+)-type capacitor electrodes (5) which are a part of the insular **silicon** layers (4). Each of the latter includes a **MOS** transistor with an n(+)-type source (81), an n(+)-type drain (82) and a **gate** insulating layer (6), in which the **gate** electrode (7) is **embedded**. Each layer (4) has two memory cells with a common drain (82); the **gate** electrodes (7) cross over the insular layers (4) and are used as word lines.

ADVANTAGE - This creates a **MOS DRAM** which is a miniaturised memory cell and is able to suppress soft errors.
1B/6

L13 ANSWER 15 OF 26 WPIX (C) 2002 THOMSON DERWENT
AN 1982-D7938E [14] WPIX
TI High density **dynamic** CMOS **memory** cell - has single transistor and capacitor cell produced in p-type bed on n-type substrate using implantation and diffusion.
DC P42 U13 U14
IN BERGLUND, C N; BOHR, M T; CHWANG, R C; YU, K K

PA (ITLC) INTEL CORP
CYC 4
PI FR 2489579 A 19820305 (198214)* 16p
JP 57083049 A 19820524 (198226)
DE 3134233 A 19820805 (198232)
US 4364075 A 19821214 (198301)
US 4409259 A 19831011 (198343)
DE 3134233 C 19910725 (199130)
PRAI US 1980-182870 19800902; US 1982-403116 19820729
AB FR 2489579 A UPAB: 19930915
The **dynamic MOS Memory** cell consists of a charge storing capacitor and a transistor formed in an n-type bed or a p-type **silicon** substrate, and is CMOS compatible. The transistor consists of a **gate** placed on top of the bed with an intermediate insulating layer, a p-type region formed in the bed under the gage and an n-type contact zone **embedded** in the p-type region and extending into the bed to couple the **gate** to the bed.

The cell may be used at high density with a high immunity to alpha particle induced soft errors. The **gate** is formed of **polysilicon** and the p-type zone is contiguous with the source-drain zone of the transistor. A dual cell consists of two p-channel transistors with a p-region divided by an n-region and coupled to two transistors. The **gate** forms the memory capacitor with the p-type zones and a supplementary capacitor is formed by the pn junctions. Wothin the **polysilicon** layer is formed a matrix of cells with capacitors and transistor control electrodes. Alpha particle immunity is provided by the stop band formed at the interface between the substrate and the n-type layer.

L13 ANSWER 16 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1999-330417 JAPIO
TI METHOD FOR ASSEMBLING **EMBEDDED DRAM** DEVICE AND THE **EMBEDDED DRAM** DEVICE HAVING DUAL **GATE** CMOS STRUCTURE
IN RIN EISHO
PA UNITED MICROELECTRONICS CORP
PI JP 11330417 A 19991130 Heisei
AI JP1998-208053 (JP10208053 Heisei) 19980723
PRAI TW 1998-107281 19980512
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 99
AB PROBLEM TO BE SOLVED: To prevent a shallow PN junction between a source/drain region and a substrate from being made still thinner by a self-aligned silicide process.
SOLUTION: An SEG process is carried out for forming plural amorphous **silicon** layers on polycrystalline **silicon** for various FETs and source/drain regions. A self-aligned silicide process is carried out on the layers to form titanium silicide layers 344, 346, 348 and 350, and the titanium silicide layers 344, 346, 348 and 350 are spaced from the substrate by source/drain regions. Since the formation of the titanium silicide layers 344, 346, 348 and 350 does not deplete the **silicon** atoms part of a substrate 300, shallow junctions causing leakage current in a **DRAM** device are prevented from being still thinner. In the case of a dual **gate** complementary **metal oxide semiconductor**(CMOS) structure, since the silicide layers are formed after the activation of impurities in the source/drain regions generation of mutual diffusion effect between an N-type polycrystalline **silicon** layer and a P-type polycrystal **silicon** layer can be prevented.

L13 ANSWER 17 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1998-079491 JAPIO
TI SEMICONDUCTOR DEVICE AND ITS MANUFACTURE
IN ITABASHI KAZUO; TSUBOI OSAMU; YOKOYAMA YUJI; INOUE KENICHI; HASHIMOTO KOICHI; NUNOFUJI WATARU
PA FUJITSU LTD, JP (CO 000522)
PI JP 10079491 A 19980324 Heisei
AI JP1997-185264 (JP09185264 Heisei) 19970710
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 98, No. 3
AB PURPOSE: TO BE SOLVED:To stably realize a **DRAM** having a high degree of integration, without deteriorating the reliability by forming a plug for connecting a storage electrode after forming a word line and by forming a storage electrode between bit lines in a self-aligned contact manner.
CONSTITUTION: xide film 11 is etched to thereby expose the surface of a substrate. A word line structure is left, a doped **silicon** layer is **embedded** in a contact hole 15, and a plug 16 for connecting a storage electrode is formed. A contact part HB of a bit line is formed, a bit line 22 is formed, and a BPSG film 26, an Si3N4 film 25, and an SiO2 film 24 are sequentially selectively removed, thereby forming a contact hole HC for the storage electrode. In a manner similar to the case for forming the contact hole 15 for the plug 16, a self alignment by the SiO2 film 24 and the Si3N4 film 25 covering the bit line structure is performed. Subsequently, a doped **silicon** layer is formed on the entire face, and a storage electrode layer 27 is formed in the contact hole HC.

L13 ANSWER 18 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1997-139475 JAPIO
TI SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS FABRICATION
IN NISHIHARA SHINJI; SUZUKI MASAYASU; SAWARA MASASHI; ISHIDA SHINICHI; ABE HIROMI; OGISHIMA JUNJI; UCHIYAMA HIROYUKI; TODA SONOKO
PA HITACHI LTD, JP (CO 000510)
PI JP 09139475 A 19970527 Heisei
AI JP1995-295220 (JP07295220 Heisei) 19951114
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 5
AB PURPOSE: TO BE SOLVED:To acquire reliable continuity of bit line connected to a memory cell selection MISFET and simultaneously reduce contact resistance of wiring connected to MISFET of peripheral circuit in a **DRAM**(**Dynamic Random** Access **Memory**) in which a memory cell of stacked capacitor structure is provided and the bit line and the first layer wiring of peripheral circuit are formed of the laminated film of W film/TiN film/Ti film.
CONSTITUTION: kness of a Ti silicide layer 35B formed on the surface of a polycrystal **silicon** plug 25 **embedded** in a connecting hole 24 for bit line BL is set to about 120nm or less to prevent separation of polycrystal **silicon** plug 25 and Ti silicide layer 35B at the interface. Moreover, thickness of the Ti silicide layer 35A formed at the surface of the p-type semiconductor region 11 of the p-channel MISFETQp of the peripheral circuit is set to about 10nm or more in order to reduce a contact resistance.

L13 ANSWER 19 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1996-023035 JAPIO
TI SEMICONDUCTOR ELEMENT AND MANUFACTURE THEREOF
IN OYU SHIZUNORI; SUDO ITSUKI; KAWAMOTO YOSHIFUMI; OKURA OSAMU; NISHIDA

TAKASHI
PA HITACHI LTD, JP (CO 000510)
PI JP 08023035 A 19960123 Heisei
AI JP1994-155636 (JP06155636 Heisei) 19940707
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 96, No. 1
AB PURPOSE: To improve an information holding characteristic of **DRAM** elements by realizing element separation corresponding to refining and preventing an increase in electric field strength.
CONSTITUTION: This semiconductor element has a structure (a) having a selective oxide film for element separation where a side near an active region 3 on a **silicon** substrate 1 is of a thin thickness t1 and a side far from it is of a thick thickness t2. The semiconductor element has also a structure (b) where the depth from the substrate surface of a high-concentration **embedded** layer 4 under the selective oxide film 2 has two kinds of d1, d2, besides the high- concentration **embedded** layer 4 near an active region where the source/drain electrodes 16 and the **gate** electrodes 17 are to be formed, has a deep depth d1 from the substrate surface. Further, the semiconductor device has a structure (c) where a layer under a thin film on the side near the active region of the selective oxide film 2 is a high-concentration **embedded** layer 5 of relatively low concentration and a layer under a thick film far from the active region of the selective oxide film 2 has a high-concentration **embedded** layer 6.

L13 ANSWER 20 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1990-159052 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR MEMORY DEVICE
IN IWASAKI YUTAKA
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 02159052 A 19900619 Heisei
AI JP1988-314031 (JP63314031 Heisei) 19881213
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 975, Vol. 14, No. 414, P. 9 (19900907)
AB PURPOSE: To minimize leakage from a charge accumulation node to a substrate and achieve a highly dense semi-**MOS dynamic memory** device by increasing the thickness of an oxide film covering the edge part near the bottom part of a groove of the charge accumulation node on the side surface of the groove formed on the substrate.
CONSTITUTION: A groove 1A is formed on a **silicon** substrate 1 and then a conductive impurities which are different from the conductive type of the substrate 1 is doped and a charge accumulation node 2 is formed. Impurities impregnating into the bottom part of the groove 1A are eliminated by adding the groove 1A and then performing etching. Then, an SiO2 film 3 is accumulated on the substrate 1, a photoresist 4 is **embedded** on it until the groove 1A is filled, and then etching is made so that the resist 4 remains from the edge part of the node 2 to 0.3.mu.m and above. Then, the SiO2 film 3 which is not coated with resist 4 eliminated and the side surface of the groove 1A of the substrate 1 is oxidized for forming an SiO2 film 5. A **polysilicon** 6 is **embedded** above it, etch-back is performed, and a cell-plate electrode is formed.

L13 ANSWER 21 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1989-025557 JAPIO
TI SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURE THEREOF
IN MENJU ATSUHIKO

PA TOSHIBA CORP, JP (CO 000307)
PI JP 01025557 A 19890127 Heisei
AI JP1987-182724 (JP62182724 Heisei) 19870722
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 759, Vol. 13, No. 213, P. 69 (19890518)
AB PURPOSE: To reduce the area occupied by a memory cell and to implement high density, in a **dynamic memory** comprising 1 transistor/1 capacitor, by using the side wall part of a trench, which is formed in an active element region of the memory cell, and side wall part of the boundary between an element isolating region of the cell and the active element region as the regions of the capacitor at the same time.
CONSTITUTION: A CVD-SiO2 film 24 is made to remain only at a peripheral part. A pattern 25 is formed at a part in contact with the film 24 by a self-aligning method. With the SiO2 24 and the resist pattern 25 as masks, a **polysilicon** film 23, an oxide film 22 and an Si substrate 21 are etched. Impurities for channel stoppers are introduced into bottom parts 26 of trenches in the Si substrate 21. Thereafter, thick oxide films 27 are formed. Thereafter, impurity regions 35 having the reverse conductivity type with respect to the substrate 21 are formed on the side wall parts of a trench 41, whose side walls become a capacitor region and holes 39. A first **gate** oxide film 28 and electrodes 29 are formed. Thereafter, **embedding** is performed with an insulating film 30, whose surface is flattened. Thereafter second **gate** oxide film 31, electrodes 32 and high concentration regions 33 and 34 are formed. Thereafter, a device is formed by an ordinary manufacturing method of **dynamic memories**.

L13 ANSWER 22 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1988-311755 JAPIO
TI **MOS** TYPE **DYNAMIC MEMORY** INTEGRATED CIRCUIT
IN INO MASAYOSHI
PA OKI ELECTRIC IND CO LTD, JP (CO 000029)
PI JP 63311755 A 19881220 Showa
AI JP1987-146982 (JP62146982 Showa) 19870615
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 743, Vol. 13, No. 155, P. 3 (19890414)
AB PURPOSE: To realize a high-capacity capacitor and a super-dense integrated circuit by a method wherein a trench is provided at a prescribed location in a substrate, the trench is filled with conducting polycrystalline **silicon**, and then a **gate** electrode is built on the conducting polycrystalline **silicon**.
CONSTITUTION: A trench 22 is provided at a prescribed location in a substrate 21, a dielectric material 2 for a capacitor is attached to the inner walls of the trench 22, conducting polycrystalline **silicon** 24 is **embedded** in the trench 22. On the entirety or a portion of the polycrystalline **silicon** 24, a **gate** electrode 29 is built, provided with a **gate** insulating film 27 on its bottom and walls 28 on its sides. Between the **gate** electrode 29 and the polycrystalline **silicon** 26, a diffusion layer 30 of the opposite conductivity type and a diffusion layer 31 of the same conductivity type are formed. A word line wiring layer 34 is formed through a contact hole 33 provided through an interlayer insulating film 32 formed on the **gate** electrode 29 and, on the word line wiring layer 34, a passivation film 35 is provided. This design enhances a capacitor in capacity and an integrated circuit in packaging density.

L13 ANSWER 23 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1988-164263 JAPIO
TI SEMICONDUCTOR DEVICE

IN ONGA SHINJI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 63164263 A 19880707 Showa
AI JP1986-308284 (JP61308284 Showa) 19861226
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 681, Vol. 12, No. 425, P. 71 (19881110)
AB PURPOSE: To obtain a **DRAM** cell, wherein a high integration density is possible, problems such as crosstalk between elements can be effectively suppressed and dispersion of element characteristics can be reduced, by laminating a transistor and a capacitor, and **embedding** the channel part of the transistor and one electrode of the capacitor in an insulating region formed in a substrate.
CONSTITUTION: In a dynamic type RAM cell comprising an **MOS** type transistor and a capacitor, said transistor and the capacitor are laminated. At least a channel part 26 of the transistor and one electrode 24 of the capacitor are **embedded** in an insulating region 21 formed in a substrate 20. For example, an oxide film 21 is formed on the **silicon** substrate 20. A groove is formed in the oxide film 21. An n- region 24, which is to become one electrode of the capacitor, and an n+ region 25, which is to become the drain of the transistor, are formed in the groove. A p- region 26, which is to become the channel part of the transistor, a **gate** oxide film 27, a **gate** electrode 28 and an n+ region 29, which is to become the source, are formed thereon. Finally, the entire surface is covered with an insulating film 30 to **embed** the **DRAM** cell completely.

L13 ANSWER 24 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1987-051249 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN HAMAMOTO TAKESHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 62051249 A 19870305 Showa
AI JP1985-189705 (JP60189705 Showa) 19850830
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 528, Vol. 11, No. 237, P. 161 (19870804)
AB PURPOSE: To prevent reduction in capacitor area and to improve the performance of a **dynamic RAM**, by making a mask material to remain on the side wall part of a groove, etching a part of an oxide film, **embedding** the oxide film at the bottom part of the groove, thereby suppressing the expansion of a **silicon** substrate at the upper part of the groove.
CONSTITUTION: On an element region, laminated films comprising poly Si 3 and a CVD SiO2 film 3' are formed. With the films as masks, a groove is formed in an element isolating region in a **silicon** substrate 1 by an RIE method. An oxide film 2 is deposited by a CVD method. Thereafter, the entire body is flattened with photoresist 2'. Then, the oxide film 2 is etched to the specified depth by the RIE method. A mask material 4 comprising a poly Si film is deposited on the entire surface. Thereafter, the entire surface is etched by using the RIE method, and a mask material 5 is made to remain on the side wall part of the groove. Then, the entire surface of the oxide film 2 is etched, and the oxide film is **embedded** in the bottom part of the groove. At this time, the mask material 5 is moved back in stead of the poly Si 3. Thereafter, the poly Si 3 is removed by the RIE, and a capacitor insulating film 6 is formed by thermal oxidation. A capacitor electrode 7 is gradually deposited, and the cell capacitor of the **dynamic RAM** is formed.

L13 ANSWER 25 OF 26 JAPIO COPYRIGHT 2002 JPO

AN 1984-224167 JAPIO
TI **MOS TYPE DYNAMIC MEMORY** AND MANUFACTURE
THEREOF
IN AZUMA TAKASHI
PA HITACHI LTD, JP (CO 000510)
PI JP 59224167 A 19841217 Showa
AI JP1983-97792 (JP58097792 Showa) 19830603
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 311, Vol. 9, No. 991, P. 35 (19850427)
AB PURPOSE: To suppress dispersion of memory capacity values, by providing a groove shaped recess part in the direction of a plate thickness along the peripheral part of the memory part in a memory region, and constituting the memory region by a substrate and a P-N junction capacitor wherein a reverse conductive type semiconductor layer is formed.
CONSTITUTION: A groove shaped recess part 11 is provided in the surface of a memory forming region surrounded by an element separating insulating layer 5 on a P type **silicon** substrate 1 in a frame shape in the direction of a plate thickness. An N- layer 2 is formed on the inner wall surface of the recess part 11. A **polysilicon** layer is **embedded** in the recess part 11 and a capacitor electrode 7 is formed. A memory region, which has the side-wall groove-shaped recess structure and comprises a P-N junction with a large contact area, is constituted. In the recess part 11, which is coated by an SiN mask 13, an Si_3N_4 layer 14 is **embedded**, and a non-memory region is formed.

L13 ANSWER 26 OF 26 JAPIO COPYRIGHT 2002 JPO
AN 1981-067953 JAPIO
TI SEMICONDUCTOR SYSTEM
IN ANAMI KENJI; TOMIZAWA OSAMU; YOSHIMOTO MASAHIKO
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 56067953 A 19810608 Showa
AI JP1979-143479 (JP54143479 Showa) 19791105
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 70, Vol. 5, No. 1291, P. 162 (19810819)
AB PURPOSE: To obtain a **dynamic RAM** strong for noises by making a value of a storage capacity great by a method wherein a semiconductor substrate, an inverse conduction type **embedded** layer and a connection area are formed and a junction area to be a capacitance is increased.
CONSTITUTION: An N type **embedded** layer 11, an N type impurity diffusion layer 12 which connects an N type diffusion or inversion layer 4 and an **embedded** layer 11 and an N type bit line diffusion layer 2 are formed on a P type semiconductor substrate 1a, 1b. And further, the 1st **polysilicon** layer 3 for the capacitor use, the 2nd **polysilicon** layer 5 for the access **gate** transistor use, and a word line electrode layer 6 are formed. With this, a storaged electrostatic capacity becomes great because a junction capacity between an **embedded** layer 11 and a impurity diffusion layer for connection and semiconductor substrate 1a, 1b is added, and on this account, a read voltage is made high, thus, a very stabilized system strong for noises being obtained.

L15 ANSWER 1 OF 2 WPIX (C) 2002 THOMSON DERWENT
AN 1995-201699 [27] WPIX
DNN N1995-158448
TI **MOS**-transistor for **e**.g. **DRAM** semiconductor memory device - has **silicon** column acting as channel region extending **perpendicular** to semiconductor substrate and surrounded by violation film and **gate** electrode.
DC U12 U13 U14
IN PARK, K; SHIM, T; YU, S; KYU-CHAN, P; SEON-IL, Y; TAE-EARN, S; SIM, T
PA (SMSU) SAMSUNG ELECTRONICS CO LTD
CYC 5

PI	DE 4430483	A1	19950601	(199527)*	20p
	FR 2713016	A1	19950602	(199527)	
	JP 07193142	A	19950728	(199539)	11p
	US 5571730	A	19961105	(199650)	19p
	US 5612559	A	19970318	(199717)	19p
	KR 141218	B1	19980715	(200018)	

ADT DE 4430483 A1 DE 1994-4430483 19940827; FR 2713016 A1 FR 1994-10372 19940829; JP 07193142 A JP 1994-179330 19940729; US 5571730 A Div ex US 1994-298470 19940830, US 1995-445649 19950522; US 5612559 A US 1994-298470 19940830; KR 141218 B1 KR 1993-25138 19931124
PRAI KR 1993-25138 19931124
AB DE 4430483 A UPAB: 19950712
The **MOS**-transistor has a **silicon** column which acts as a channel region. The **silicon** column extends **perpendicular** to a semiconductor substrate of first conductivity type and is surrounded by an isolation film. A **gate** electrode (33) surrounds the **silicon** column.

A **gate** isolation film (30) is between the column and the **gate** electrode. A first interference point region (12) and a second interference point region (28), both of a second conductivity type are arranged in the lower region of the column.

ADVANTAGE - Requires small area allowing high integration density in associated semiconductor device.
Dwg.1/17

L15 ANSWER 2 OF 2 JAPIO COPYRIGHT 2002 JPO
AN 1992-218954 JAPIO
TI SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND ITS MANUFACTURE
IN MATSUMOTO SUSUMU; YABU TOSHIKI; NAKADA YOSHIRO; MATSUO NAOTO; OKADA SHOZO
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 04218954 A 19920810 Heisei
AI JP1991-75041 (JP03075041 Heisei) 19910408
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1296, Vol. 16, No. 567, P. 94 (19921208)
AB PURPOSE: To provide a semiconductor integrated circuit device composed of **DRAM** having a capacitor cell capable of obtaining a high charge capacity in a small region without being influenced by the minimum dimensions regulated by a lithography and also provide the manufacture of the integrated circuit device.
CONSTITUTION: A **MOS** transistor for memory cell is composed of a source region 3, a drain region 4, a **gate** oxide film 11a and a **gate** electrode (word line) 5 which are formed on the surface of a semiconductor substrate 1. A capacitor cell for memory cell is composed of a charge-storage electrode 8, a capacity insulation film 9 and a plate electrode 10 and its charges are stored in the charge-storage electrode 8. A bit line 6 is composed of a composite film of **polysilicon** film 16a and a high melting-point metal silicide film 17a. According to this

constitution, the title device has an **upright** double frame-shaped part on the base of the charge-storage electrode 8 and the surface of the frame- shaped part is also used as a capacitor so that the surface area of the capacitor is made larger and higher charge capacity can be obtained in the same area as that of a hitherto known stacked capacitor cell.

L18 ANSWER 1 OF 8 WPIX (C) 2002 THOMSON DERWENT
AN 1999-119909 [10] WPIX
DNN N1999-087528 DNC C1999-034937
TI Fabrication of complementary **metal oxide semiconductor** (CMOS) and **dynamic** access **memory** (**DRAM**) devices - on the same semiconductor chip with only two additional masking steps.
DC L03 U11 U13 U14
IN SUNG, J
PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
CYC 1
PI US 5858831 A 19990112 (199910)* 28p
ADT US 5858831 A US 1998-31683 19980227
PRAI US 1998-31683 19980227
AB US 5858831 A UPAB: 19990310
CMOS and **DRAM** devices are formed on a single semiconductor chip by; (a) Providing areas on the substrate to be used for logic (50) and memory (60) devices. (b) Forming P (2) and N (4) well regions in the logic area to be used with N and P channel logic devices respectively. (c) Forming a P well in the memory area to be used with N channel memory devices. (d) Forming **gate** insulator layers (7) (8) in logic and memory areas. (e) Forming insulator filled trenches to isolate the logic P and N wells, and the logic and memory areas. (f) Forming a polycide **gate** structures (16,17,18) (metal silicide / titanium nitride / **polysilicon**) over the first (N type **polysilicon**) and second (P type **polysilicon**) logic regions, and the memory area (N type **polysilicon**). (g) Forming **silicon** nitride spacers (20b) on the **gate** structures in the two logic regions. (h) Forming N and P lightly (23) and heavily (24) doped source and drain regions in the two logic regions in areas not covered by the **gate** structure. (i) Forming metal silicide (28) on the heavily doped source and drain regions of the logic devices, and insulator plugs (29) between the **gate** structures. (j) Forming **silicon** nitride spacers (20b) on the **gate** sides, N type lightly doped source and drain (31), and **polysilicon** plugs (33) between the **gate** structures overlying and contacting the source and drain regions in the memory area. (k) Depositing an insulator layer (34), and forming a storage node opening (36) exposing the **polysilicon** plugs in the memory area. (l) Forming a capacitor structure (37,38) in the node opening overlying and contacting the **polysilicon** plugs. (m) Forming a metal contact structure (44,45,46) to the capacitor in the memory area, to the N type heavily doped source and drain in the first logic area and to the P type heavily doped region in the second logic area.

USE - **DRAMs** and CMOS devices.

ADVANTAGE - The combination of a **high performance** logic device and a low cost memory device on a single chip is achieved with the addition of only two masking steps.
Dwg.20/20

L18 ANSWER 2 OF 8 WPIX (C) 2002 THOMSON DERWENT
AN 1991-281006 [38] WPIX
CR 1986-206120 [32]; 1992-202085 [25]; 1993-242480 [30]
DNN N1991-214802
TI Extended silicide and external contact technology - permits manufacture of **high performance** bipolar and **high performance MOS** devices on same integrated circuit die.
DC U11 U13
IN BURTON, G N; KAPOOR, A K; VORA, M B

PA (FAIH) FAIRCHILD SEMICONDUCTOR CORP
CYC 1
PI US 5045916 A 19910903 (199138)*
ADT US 5045916 A US 1989-383245 19890719
PRAI US 1985-693062 19850122; US 1986-817231 19860108; US 1989-383245 19890719
AB US 5045916 A UPAB: 19931118
There is disclosed a process for making **high performance** bipolar and **high performance MOS** devices on the same integratred circuit die. The process comprises forming isolation islands of epitaxial **silicon** surrounded by field oxide and forming **MOS** transitors having **polysilicon gates** in some islands and forming bipolar transistors having **polysilicon** emitters in other islands. Insulating spacers are then formed around the edges of the **polysilicon** electrodes by anisotropically etching a layer of insulation material, usually thermally grown **silicon** dioxide covered with additional oxide deposited by CVD.

A layer of refractory metal, preferably titanium covered with tungsten, is then deposited and heat treated at a temperature high enough to form only titanium disilicide to form silicide over the tops of the **polysilicon** electrodes and on top of the bases, sources and drains. Regions of this refractory metal are then masked off such that the refractory metal extendsa to a contact pad position external to the isolation island. Metal posts can be formed at the contact pad positions and a layer of planarized insulation material is formed so to leave only the tops of the posts exposed. A layer of metal can then be deposited and etched to make electrical contact with tops of the posts.

ADVANTAGE - Minimises area consumed by cell. @(35pp Dwg.No.2/35)@

L18 ANSWER 3 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1997-321242 JAPIO
TI SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND MANUFACTURE THEREOF
IN AOKI HIDEO; TADAKI YOSHITAKA; SEKIGUCHI TOSHIHIRO
PA HITACHI LTD, JP (CO 000510)
PI JP 09321242 A 19971212 Heisei
AI JP1996-136318 (JP08136318 Heisei) 19960530
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 12
AB PURPOSE: TO BE SOLVED:To advance the improvement for providing a high speed, **high performance** and high integration degree device by simplifying the process of manufacturing a **DRAM** having a capacitor over bit line structure.
CONSTITUTION: contained conductive film having a lower resistance than that of a **polysilicon** or polycide is used to form **gate** electrodes 8A (word lines WL) of memory cell selecting MISFETs Qt, and **gate** electrodes 8B and 8C of n-and p-channel type MISFETs Qp for peripheral circuits in the same step. A W-contained conductive film is used to form bit lines BL1, BL2 and wirings 30A, 30B on a second layer of the peripheral circuits in the same step.

L18 ANSWER 4 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1995-142607 JAPIO
TI SEMICONDUCTOR MEMORY AND MANUFACTURING METHOD THEREOF
IN MORIHARA TOSHINORI
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 07142607 A 19950602 Heisei
AI JP1994-157390 (JP06157390 Heisei) 19940708
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No.

6

AB PURPOSE: To easily obtain a high integrated structure having **high performance** in an SOI structured **DRAM**.
CONSTITUTION: A dielectric layer 2 is formed on the main surface of a semiconductor substrate 1. A **silicon** layer 3 is formed on the dielectric layer 2. **MOS** transistors 9a, 9b are formed on the **silicon** layer 3. The **MOS** transistor 9a is provided with impurity regions 8c, 8b in the semiconductor layer 3. A capacitor 15 is composed of this impurity region 8c, the dielectric layer 2 and the semiconductor substrate 1. Furthermore, the dielectric layer 2 also functions as the SOT structured insulating film.

L18 ANSWER 5 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1987-293759 JAPIO
TI SEMICONDUCTOR DEVICE
IN AKIYAMA SHIGENOBU; OSONE TAKASHI
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 62293759 A 19871221 Showa
AI JP1986-138562 (JP61138562 Showa) 19860613
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 616, Vol. 12, No. 189, P. 111 (19880602)
AB PURPOSE: To realize large scale integration and improved performance of a semiconductor device by a method wherein polycrystalline Si which fills trenches formed in an Si substrate is used as storage capacitor electrodes and SOI-Si layers which are formed with apertures on the substrate surrounded by the capacitor electrodes as seeds are recrystallized to form switching transistors.
CONSTITUTION: Trenches which are formed in an Si substrate 1 composed of a P+type Si substrate 1A and a P-type Si epitaxial layer are filled with polycrystalline Si 3 with insulating films 2 and 4 there between. SOI (**Silicon** on Insulator) recrystallized Si layers 5 are formed with the parts 1B of the Si substrate 1 as seeds and the SOI-Si layers 5B directly above the parts 1B are empolyed as channel regions of switching transistors Moreover, a part of one of N+type regions 5A of the source and drain of the switching transistor and a part of a storage capacitor electrode 3 are in direct contact with each other and the other N+type region of the source or drain is made to be common with the source or drain of one of the adjoining switching transistors to form a bit line 7. With this constitution, a **DRAM** or the like with high integrity and **high performance** can be obtained.

L18 ANSWER 6 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1984-113659 JAPIO
TI **MOS DYNAMIC MEMORY**
IN OGURA ISAO; HORIGUCHI FUMIO
PA TOSHIBA CORP, JP (CO 000307)
PI JP 59113659 A 19840630 Showa
AI JP1982-223446 (JP57223446 Showa) 19821220
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 274, Vol. 8, No. 2311, P. 98 (19841024)
AB PURPOSE: To eliminate contact holes, to dissolve the problem of contact resistance, to simplify the manufacturing process and to obtain an **MOS dynamic memory** of **high performance** at low cost by a method wherein the combination **gate** electrode and word line of a switching transistor is formed.
CONSTITUTION: After an Si3N4 film pattern, an oxide film pattern, N+ type impurity regions 6, 7, etc., are formed in order on the surface of a P type **silicon** substrate 1, a thermally oxide film 12 is formed thick on the surface of a polycrystalline **silicon** pattern 11 and

thin on the surface of the substrate 1. At this time, phosphorus is thermally diffused from the **silicon** pattern 11 to form an N+ type impurity region 13 under the drain region 7. Then after an Al film is evaporated on the whole surface, patterning is performed to form the **gate** electrode 14 of a switching transistor to be used both as a word line. Then a protective film is coated on the whole surface to manufacture an **MOS dynamic memory**. At the **MOS dynamic memory** thereof, the channel length direction of the switching transistor and the wiring direction of the word line are formed making the angle of 45 degrees. When the angle thereof is in the extent of 30- 60 degrees, a high degree of integration can be held.

L18 ANSWER 7 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1984-013365 JAPIO
TI **METAL OXIDE SEMICONDUCTOR DYNAMIC MEMORY** AND ITS MANUFACTURE
IN OGURA ISAO
PA TOSHIBA CORP, JP (CO 000307)
PI JP 59013365 A 19840124 Showa
AI JP1982-122475 (JP57122475 Showa) 19820714
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 242, Vol. 8, No. 951, P. 63 (19840502)
AB PURPOSE: To obtain the high integration-degree **high-performance MOS dynamic memory**, in which a short-channel effect does not affect and effective channel length does not vary and a value in conformity with a design is obtained in the threshold voltage of a switching transistor, by forming the switching transistor through self-alignment.
CONSTITUTION: A field oxide film 32 is formed to a P type **silicon** substrate 31, and a thin thermal oxide film 33 is formed to the surface of the substrate 31. An N+ type impurity region 34 is formed in a memory cell region, and a first layer polycrystalline **silicon** film 35 and a first CVD-SiO2 film 36 are deposited on the whole surface in succession. These deposit layers are removed through selective etching, and the N+ type impurity region 34 exposed from the etching region is removed through etching in the junction depth or more to form groove sections 37, 37. First and second N+ type impurity regions 38, 38, 39 isolated by the groove sections 37, 37 are formed, second **gate** oxide films 46, 46 are formed through thermal oxidation treatment, and **gate** electrodes 47, 47 are formed onto the oxide films 46, 46, thus forming the switching transistor through self-alignment.

L18 ANSWER 8 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1980-086147 JAPIO
TI MANUFACTURE OF **MOS DYNAMIC MEMORY** ELEMENT
IN OGURA ISAO
PA TOSHIBA CORP, JP (CO 000307)
PI JP 55086147 A 19800628 Showa
AI JP1978-158710 (JP53158710 Showa) 19781225
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 26, Vol. 4, No. 1331, P. 70 (19800918)
AB PURPOSE: To provide a **MOS dynamic memory** element of **high performance** and high efficiency by forming, on a high resistance semiconductor substrate whose impurity concentration is specified, an oxide film whose thickness is also specified, to obtain multi-layer **gate** construction, and providing a high concentration region in the substrate adjoining the multi-layer.
CONSTITUTION: On a p-type **silicon** substrate 11 whose impurity

concentration is specified within 5.times.1014/cm2, a thick element separating silica film 12 is formed, and on the part of the substrate 11 surrounded by the film 12, a thin silica film 13 whose thickness is limited within 500.ANG. is coated. Next, covering from the center of this film 13 to one side of the film 12, the first polycrystalline **silicon** film 14 is formed, to form a **MOS** capacitor 15, the exposed part of the film 13 is removed, and there, a p+-type region adjoining the film 14 is diffusion-formed. Next, on this region 17, a **gate** silica film 18 whose thickness is also within 500.ANG. is coated, and on the film above the film 13, an insulating silica film 19 and the second polycrystalline **silicon** film 20 are deposited, and the part above the region 17 is used as a **MOS** transistor 16. Next, an n-type drain region 21 is diffusion-formed adjoining the region

L21 ANSWER 1 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 2002-416762 [44] WPIX
DNN N2002-327955
TI Sense amplifier for use with a **dynamic random** access **memory** (**DRAM**), the pitch (lateral size) of the sense amplifiers is made to match the pitch of the smallest memory cells using U-shaped **gate** design and offset transistor rows.
DC U13 U14
IN LEHMANN, G; LEIDINGER, T; REITH, A M; REITH, A
PA (INFN) INFINEON TECHNOLOGIES AG; (INFN) INFINEON TECHNOLOGIES NORTH AMERICA CORP
CYC 22
PI WO 2002029894 A2 20020411 (200244)* EN 47p
RW: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE TR
W: JP KR
US 6404019 B1 20020611 (200244)
ADT WO 2002029894 A2 WO 2001-US27143 20010830; US 6404019 B1 US 2000-676870 20000929
PRAI US 2000-676870 20000929
AB WO 200229894 A UPAB: 20020711
NOVELTY - A sense amplifier is formed in a **silicon** integrated circuit. The pitch of an array of such amplifiers is equal to the pitch of **pairs** of bit lines (150) of a memory array. Each array of amplifiers is formed from four rows of transistors of an n or p- channel type **MOS** transistor with a U-shaped **gate** electrode. The **gate** electrode of the transistors in each row of transistors of the amplifier is offset from those in a previous row by a pre-selected amount. The bit lines are straight.

USE - With **dynamic random** access **memory** fabricated in semiconductor integrated circuits

ADVANTAGE - Allows support circuits, such as sense amplifiers, to be designed with a width commensurate with the width of the memory cells, has a simple repetitive structure, cost effective, does not introduce extra capacitance onto the bit lines

DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a prior art memory circuit which can be used in conjunction with the invention.
Memory cells 110
Top array 120
Bottom array 130
Word lines 140
Bit lines 150
Dwg.1/8

L21 ANSWER 2 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 2002-280051 [32] WPIX
DNN N2002-218702 DNC C2002-082311
TI Nonvolatile memory cell, e.g. non volatile random access memory, has vertical electrical via which couples plate of capacitor through insulator layer to **gate** of transistor.
DC L03 U11 U13
IN CLOUD, E H; NOBLE, W P
PA (CLOU-I) CLOUD E H; (NOBL-I) NOBLE W P; (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 2002024083 A1 20020228 (200232)* 20p
US 6380581 B1 20020430 (200235)
ADT US 2002024083 A1 US 1999-259493 19990226; US 6380581 B1 US 1999-259493 19990226

PRAI US 1999-259493 19990226
AB US2002024083 A UPAB: 20020521
NOVELTY - Nonvolatile memory cell (200A-200B) comprises transistor (210A-210B), a capacitor (220A-220B), and a vertical electrical via (230A-230B). The via couples a first plate (223) of the capacitor through an insulator layer (232) to **gate** (212A-212B) of the transistor.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for:

(I) a non volatile memory array (200) comprising the above-mentioned non volatile memory cells, a **wordline** coupled to the top plate of the stacked capacitor, a bit line (219A-219B) coupled to a drain region (216A-216B) of **metal oxide semiconductor** field effect transistor (MOSFET), and a sourceline (217A-217B) coupled to a source region (215A-215B) of the MOSFET;

(II) an electronic system comprising a processor, a **dynamic random** access **memory** (**DRAM**) chip, and a system bus coupling the processor to the **DRAM** chip;

(III) a method for forming a non volatile memory cell on a **DRAM** chip comprising forming a MOSFET in a substrate on the **DRAM** chip, forming a stacked capacitor above the **gate** of the MOSFET using a **DRAM** process, and forming an electrical contact using a **DRAM** process;

(IV) a method of operating a memory cell comprising controlling a charge on the **gate** of MOSFET and on the bottom plate of the capacitor to regulate a threshold voltage for the memory cell; and

(V) a method of programming a memory device comprising grounding a source region for MOSFET, applying a control **gate** voltage to the top plate, and applying a drain voltage of approximately half of the control **gate** voltage to a drain region of the MOSFET.

USE - Used as non volatile access memory, e.g. electrically erasable and programmable read only memory, or a flash memory cell (claimed).

ADVANTAGE - Operates with lower programming voltages than that used by conventional non volatile memory cells, yet still hold sufficient charge to withstand the effects of parasitic capacitances and noise due to circuit operation, thus realizing the requirements of low power density packed integrated circuits for smaller, portable devices.

DESCRIPTION OF DRAWING(S) - The drawing shows a perspective view of a non volatile memory array.

memory array 200
nonvolatile memory cell 200A-200B
transistor 210A-210B
gate 212A-212B
source region 215A-215B
drain region 216A-216B
sourceline 217A-217B
bit line 219A-219B
capacitor 220A-220B
plate 223
electrical via 230A-230B
insulator layer 232
Dwg.2/8

L21 ANSWER 3 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 2001-380454 [40] WPIX
DNN N2001-278907 DNC C2001-116465
TI Formation of self-aligned contact to semiconductor element in **metal oxide semiconductor** field effect transistor by etching insulative layers using etchant mixture of octafluorocyclobutane, fluoromethane, and oxygen in argon carrier gas.
DC L03 U11

IN CHEN, B; JENG, E S
PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
CYC 1
PI US 6239011 B1 20010529 (200140)* 12p
ADT US 6239011 B1 US 1998-89557 19980603
PRAI US 1998-89557 19980603
AB US 6239011 B UPAB: 20010719

NOVELTY - A self-aligned contact is formed to a semiconductor element adjacent to a **gate** electrode of a metal-oxide-**silicon** -field-effect-transistor by etching first and second insulative layers (29) in a reactive ion etching tool in an radiofrequency (rf) plasma containing an etchant mixture of octafluorocyclobutane and fluoromethane, in an argon carrier gas, while adding a flow of oxygen.

DETAILED DESCRIPTION - Formation of self-aligned contact to a semiconductor element adjacent to a **gate** electrode of a metal-oxide-**silicon**-field-effect-transistor (MOSFET), involves:

(a) providing **silicon** wafer having vertical walled **gate** stack with a **silicon** nitride insulative cap, a **silicon** nitride sidewall, and an active semiconductor element within the surface of the **silicon** wafer adjacent the sidewall;

(b) depositing a first insulative layer over the wafer;

(c) depositing a second insulative layer on the first insulative layer;

(d) planarizing the second insulative layer;

(e) depositing a photoresist layer over the second insulative layer;

(f) patterning the photoresist layer to define a contact opening which extends over the sidewall and partially over the cap; and

(g) etching the first and second insulative layers to form a contact opening (40) that is aligned to the sidewall;

(h) removing residual polymer and photoresist layer; and

(i) depositing a conductive material into the contact opening to form a self-aligned contact (42).

In step (g), the insulative layers are etched in a reactive ion etching tool in an rf plasma containing an etchant mixture, at a flow rate to maintain a chamber pressure of 2-10 millitorr, while adding a flow of oxygen (O_2) to maintain and control steady state thickness of a polymer (36) which forms on surfaces of the cap and sidewall exposed by the etching. The etchant mixture is octafluorocyclobutane and fluoromethane, in an argon carrier gas. Etching is carried out to achieve a **silicon** oxide/**silicon** nitride etch rate ratio of 20:1, while not obstructing the etching by polymer bridging.

An INDEPENDENT CLAIM is also included for a method of forming a **dynamic random** access **memory (DRAM)** cell involving, providing a **silicon** wafer having a **gate** oxide layer subjacent to a conductive layer; depositing a **silicon** oxide layer over the conductive layer; depositing a first **silicon** nitride layer over the **silicon** oxide layer; depositing and patterning a first photoresist layer to define **two** adjacent **wordlines**; anisotropically etching the **silicon** nitride layer, **silicon** oxide layer, and conductive layer to form **wordlines**; implanting a first dose of impurity atoms; removing the first photoresist layer; depositing a second **silicon** nitride layer; anisotropically etching the second **silicon** nitride layer to form sidewalls along the edges of the **wordlines**; implanting a second dose of impurity atoms to form a semiconductive element; performing steps (c)-(e) of the method for forming self-aligned contact to a semiconductor element adjacent to a **gate** electrode of a MOSFET; patterning the second photoresist layer to define a bitline contact opening between **two** adjacent **wordlines** where the

bitline contact opening is to be self-aligned to the sidewalls; performing steps (g)-(i) of the method for forming self-aligned contact to a semiconductor element adjacent to a **gate** electrode of a MOSFET; forming a bitline over the bitline contact; and forming storage capacitors on the **silicon** wafer.

USE - The method is used for forming contacts in the manufacture of sub-micron MOSFET used in **DRAM** cell.

ADVANTAGE - Addition of O2 in small amounts reduces the encroachment of polymer into the narrower opening, thus preventing pinch-off. Small amounts of O2 also improve the ability to etch stop on the **silicon** nitride interfaces, thus reducing the risk of **gate**-to-bitline contact shorts.

DESCRIPTION OF DRAWING(S) - The figures show a sectional view of a portion of **DRAM** cell upon completion of the etching step and a sectional view of the **DRAM** cell after depositing a contact into the self-aligned contact opening.

Insulative layer 29
Residual polymer 36
Contact opening 40
Contact 42
5e, 5f/5

L21 ANSWER 4 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 2000-548295 [50] WPIX
DNN N2000-405594 DNC C2000-163582
TI Metal/barrier/**silicon** stack structure formation tungsten-poly **gate** structure, involves heat treating stack to transform nitride into conductive barrier between metal and **silicon**.
DC L03 U11
IN ANDERSON, D N; CARTER, D E; HSU, W; HWANG, M; LU, J
PA (TEXI) TEXAS INSTR INC
CYC 1
PI US 6100188 A 20000808 (200050)* 5p
ADT US 6100188 A Provisional US 1997-51798P 19970707, US 1998-108474 19980701
PRAI US 1997-51798P 19970707; US 1998-108474 19980701
AB US 6100188 A UPAB: 20001010

NOVELTY - A metal/barrier/**silicon** stack structure is formed by:
(a) depositing a **silicon** layer (30) on a substrate (32);
(b) forming a **silicon** nitride layer;
(c) depositing a metal layer to form a metal/nitride/**silicon** stack; and
(d) heat treating the stack to transform the nitride into a conductive barrier layer between the metal and **silicon**.

USE - For forming a metal/barrier/**silicon** stack structure useful in forming a tungsten-poly **gate** structure (claimed). The tungsten-poly **gate** structure can be used in microelectronic devices requiring metal-poly **gates**, e.g. fabrication of low-resistance **wordlines** for **dynamic random** access **memory** devices and **gates** for complementary **metal oxide semiconductor** logic devices.

ADVANTAGE - The barrier layer blocks reaction between tungsten and **silicon**, enhances sheet resistance, enhances adhesion between tungsten and the poly, and is stable at high temperatures. The process is time-efficient with a resulting high effective throughput. The **gate** structures can use selective oxidation to remove etching damage to **gate** oxide. The invention reduces the thermal budget as compared to existing stack processes.

DESCRIPTION OF DRAWING(S) - The figure shows a schematic view of the invention.

Silicon layer 30
Substrate 32
Tungsten 36
Conductive barrier 38
Dwg.5/5

L21 ANSWER 5 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 2000-490182 [43] WPIX
DNN N2000-363731 DNC C2000-147182
TI Manufacture of **dynamic random** access **memory** capacitor involves etching the oxide layers, and portions of mask layer and insulating layer to form contact window using self-aligned etching process.
DC L03 U11 U12 U13 U14
IN HUNG, Y; HONG, G
PA (UNMI-N) UNITED MICROELECTRONICS CORP; (UNSE-N) UNITED SEMICONDUCTOR CORP
CYC 2
PI US 6087218 A 20000711 (200043)* 8p
TW 407376 A 20001001 (200132)
ADT US 6087218 A US 1998-54836 19980403; TW 407376 A TW 1997-118765 19971212
PRAI TW 1997-118765 19971212
AB US 6087218 A UPAB: 20000907

NOVELTY - A **dynamic random** access **memory** (**DRAM**) capacitor is manufactured by etching the second oxide layers, a portion of first oxide layer, and portions of mask layer and insulating layer to form contact window in the insulating layer using a self-aligned etching process.

DETAILED DESCRIPTION - Manufacture of **DRAM** capacitor comprises providing a semiconductor substrate having **MOS** transistor(s) formed on the substrate (30). The **MOS** transistor has a **gate** that acts as a **word line** and source/drain terminals in the substrate on each side of the **gate** terminal. The **polysilicon** layer (33, 41a) between the transistor **gate** is patterned to act as a bit line (37), and the bit line is electrically coupled to one source/drain terminal of the **MOS** transistor. An insulating layer is formed over the substrate, the **word line** and the bit line. The mask layer (39a), first oxide layer and the first **polysilicon** layer are formed over the insulating layer (38). An opening is formed in the first **polysilicon** layer located directly above a source/drain region (36a, 36b). A second oxide layer is formed over the first **polysilicon** layer and the opening where the second layer forms a groove in the opening. The second oxide layer, a portion of the mask layer, a portion of the first oxide layer and a portion of insulating layer are etched to form a contact window in the insulating layer using a self-aligned etching process. A second **polysilicon** layer (46) is deposited over the first **polysilicon** layer and into the contact window to form electrical connection with the source/drain region. The first and second **polysilicon** layers are patterned, then the first oxide layer is removed. The first and second **polysilicon** layers act together as a lower electrode of the capacitor. A dielectric layer (48) is formed over the first and second **polysilicon** layers, then a third **polysilicon** layer (49) is formed over the dielectric layer to act as an upper electrode capacitor.

USE - For the manufacture of **DRAM** capacitor.

ADVANTAGE - The invention provides a self-aligned processing method that is free from the limitations imposed by the resolution of light source.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view

showing the progression of the manufacture of **DRAM** capacitor.
Substrate 30
Structures 31
Polysilicon layers 33, 41a, 46, 47, 49
Source/drain regions 36a, 36b
Bit line 37
Insulating layer 38
Mask layer 39a
Dielectric layer 48
Dwg.3G/3

L21 ANSWER 6 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 2000-295380 [26] WPIX
DNN N2000-221652
TI **Dynamic memory** cell with addressing commutation, comprising a capacitor with first terminal connected to the bit line via a transistor, and second terminal connected to a supplementary row line.
DC U13 U14
IN FERRANT, R
PA (SGSA) STMICROELECTRONICS SA
CYC 1
PI FR 2784493 A1 20000414 (200026)* 18p
ADT FR 2784493 A1 FR 1998-12843 19981009
PRAI FR 1998-12843 19981009
AB FR 2784493 A UPAB: 20000531
NOVELTY - The memory cell for an integrated circuit memory unit comprises a transistor (T) of **MOS** (metal-oxide-**silicon**) type for selection, and a capacitor (C) with the first terminal (SN) connected via the transistor to the bit line (2). The **gate** (G) of the transistor is connected to the **word line** (1), and the second terminal of the capacitor is connected to a supplementary row line (3), which potential varies according to the addressing of the corresponding **word line**.

DETAILED DESCRIPTION - The source (S) of the transistor (T) is connected to the first terminal (SN) of the capacitor (C), and the drain (D) to the bit line (2). The voltage level in the memory cell is determined by the potential of the row line (3) during the period of addressing the cell. The **word line** (1) is addressable between **two** potentials which do not exceed the supply potentials of the memory circuit, e.g. Vdd and zero, that of the ground. The addressing procedure includes a change of the potential of the second terminal of the capacitor, and the stationary potential is intermediate between the **two** supply potentials, e.g. equal to Vdd/2. The addressing potential at the second terminal of the capacitor corresponds to a supply potential.

USE - In integrated circuit memory units with memory cells in matrix, in particular in **dynamic random** access **memory** (**DRAM**) units.

ADVANTAGE - Possible operation at a lower supply voltage with reduced harmful effects on the lifetimes of transistors, and avoids drawbacks of a charge pump circuit; resolves problem of writing a higher state without erasing a lower state.

DESCRIPTION OF DRAWING(S) - The drawing is a circuit diagram of the memory cell.
Word line 1
Bit line 2
Row line 3
Capacitor C
Transistor T

Dwg.3/4

L21 ANSWER 7 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1998-278092 [25] WPIX
DNN N1998-219000
TI Semiconductor memory **e**.g. **DRAM** - has p-**silicon** germanium layer, whose energy difference between valence band and vacuum level is smaller than that between balance band and vacuum level of p-**silicon** layers.
DC U12 U13 U14
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 10092952 A 19980410 (199825)* 9p
ADT JP 10092952 A JP 1996-246710 19960918
PRAI JP 1996-246710 19960918
AB JP 10092952 A UPAB: 19980624

The memory comprises an n-channel **MOS** transistor having **double** heterojunction structure under the channel area. A **word line** (WL) and the source of the **MOS** transistor are connected to a bit line (BL). The drain and **gate** of the **MOS** transistor are connected to a power supply line (VL).

The **double** heterojunction structure consists of a first p-**silicon** layer (3), a p-**silicon** germanium layer (4) and a second p-**silicon** layer (5) formed respectively on a **silicon** substrate (1). The energy difference between the valence band and vacuum level of the p-**silicon** germanium layer is smaller than that between the valence band and vacuum level of the p-**silicon** layer.

ADVANTAGE - Has simplified structure. Attains high integration.

Dwg.2/8

L21 ANSWER 8 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1997-185709 [17] WPIX
DNN N1997-153222
TI **DRAM** mfg method - involves connecting N-type source-drain area to storage- node electrode through node-contact hole made in first interlayer insulating film.
DC U13 U14
PA (NIDE) NEC CORP
CYC 1
PI JP 09045875 A 19970214 (199717)* 19p
ADT JP 09045875 A JP 1995-193568 19950728
PRAI JP 1995-193568 19950728
AB JP 09045875 A UPAB: 19970424

The method involves forming a **MOS** transistor with N-type source-drain access (114B) and a **gate** electrode formed through a **gate** oxide film (112) on a P-type **silicon** substrate (101) in a **word line** (113). A memory cell (103) is formed by stacking storage-node electrode (128) consisting of a first conductive material film pattern (129), a capacitive insulating film (131) and a cell-plate electrode of capacitive element. The element for characteristic measurements contains a conductive material film and a second conductive material film pattern. The surface of the **MOS** transistor formed is covered by a first inter layer insulating film (116) in which node-contact holes. Then, the bit line and the first inter layer insulating film are covered by a second inter layer insulating film (121) containing **silicon** oxide or **silicon** nitride film.

The storage-node electrode is connected to the source-drain area through second node-contact hole formed in the first inter laying

insulating film. A space is given between the base of storage- node electrode and upper face of second interlayer insulating film narrower than space between **two** storage-node electrodes. A second conductive material film pattern is formed over upper face of second inter layer insulating film.

ADVANTAGE - Prevents short circuit between memory cells. Enables to measure characteristic of storage-node electrode.

Dwg.3/17

L21 ANSWER 9 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1993-046242 [06] WPIX
DNN N1993-035394 DNC C1993-020853
TI Increased density of **dynamic RAM** storage cell - uses trench capacitors separated by the length of the access transistor **gate** with diffusion contacts made vertically in.the top of the trench.
DC L03 U13 U14
IN MELZNER, H
PA (SIEI) SIEMENS AG
CYC 18
PI DE 4125199 A1 19930204 (199306)* 11p
WO 9303501 A1 19930218 (199309) DE 30p
RW: AT BE CH DE DK ES FR GB GR IT LU MC NL SE
W: JP KR US
DE 4125199 C2 19940428 (199415) 11p
EP 596975 A1 19940518 (199420) DE
R: AT DE FR GB IT NL
JP 06509443 W 19941020 (199501) 7p
US 5378907 A 19950103 (199507) 12p
EP 596975 B1 19951206 (199602) DE 18p
R: AT DE FR GB IT NL
DE 59204621 G 19960118 (199608)
IE 80400 B 19980617 (199833)
KR 273779 B 20001215 (200174)
ADT DE 4125199 A1 DE 1991-4125199 19910730; WO 9303501 A1 WO 1992-EP1653 19920720; DE 4125199 C2 DE 1991-4125199 19910730; EP 596975 A1 EP 1992-916425 19920720, WO 1992-EP1653 19920720; JP 06509443 W WO 1992-EP1653 19920720, JP 1993-503215 19920720; US 5378907 A WO 1992-EP1653 19920720, US 1994-182187 19940126; EP 596975 B1 EP 1992-916425 19920720, WO 1992-EP1653 19920720; DE 59204621 G DE 1992-504621 19920720, EP 1992-916425 19920720, WO 1992-EP1653 19920720; IE 80400 B IE 1992-2466 19920729; KR 273779 B WO 1992-EP1653 19920720, KR 1994-700278 19940128
FDT EP 596975 A1 Based on WO 9303501; JP 06509443 W Based on WO 9303501; US 5378907 A Based on WO 9303501; EP 596975 B1 Based on WO 9303501; DE 59204621 G Based on EP 596975, Based on WO 9303501; KR 273779 B Previous Publ. KR 94702007, Based on WO 9303501
PRAI DE 1991-4125199 19910730
AB DE 4125199 A UPAB: 19930924
The semiconductor storage device consists of a substrate (1) in which trenches (7) have been formed. Inside the trench a first electrode (12), an insulation layer (14) and a second electrode (16) constitute the capacitor. The first electrode (12) is insulated from the substrate by an insulating layer (8,9) except for a buried contact (11) near the top of the trench on one side, which forms the source (15) of the access transistor. At the opposite side the first electrode stops well short of the top of the trench, to allow the bitline contact to be formed in the trench wall, which forms the drain of the access transistor. The second electrode (16) is insulated from the bitline (20,21) by an insulating layer (17), pref. made by oxidation of the **polysilicon** layer

(16), and a top layer (18) which is pref. made by decomposition of TEOS (tetraethylorthosilicate). The trench is self-aligned w.r.t. the **gate** (4) of the access transistor, the **gate** of the access transistor of the next cell and the field oxide regions (2) which run parallel to the rows of cells. The capacitor (12,14,16) follows the inner contours of the trench. The insulating layer (8,9) pref. is a **double** layer of Si-oxide (8) and Si-nitride (9).

USE/ADVANTAGE - The design allows further densification which makes it suitable for the mfr. of 64Mbit **DRAMs**. The cell area has been reduced without reducing the capacitor area. A cell occurs at each point where the **wordline** and bitline cross. The process uses self alignment, allowing less dependence on the lithographic process. Cell dimensions are typically: **wordline** pitch: 2.1 micron, **wordline** width: 0.7 micron, bitline pitch: 1.4 micron, width 0.7 micron. Trench size 0.7 x 1.4 micron, depth 3 micron. The cell area is 2.94 micron.
7/9

L21 ANSWER 10 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1988-176633 [26] WPIX
DNN N1988-135019
TI High density **VMOS dynamic RAM** array - has trench capacitor, and single access transistor with **gate** connected to **word line** and drain connected to bit line.
DC U11 U13 U14
IN HWANG, W; SCHUSTER, S E; TERMAN, L; TERMAN, L M
PA (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP
CYC 6
PI EP 272476 A 19880629 (198826)* EN 11p
R: DE FR GB IT
JP 63157463 A 19880630 (198832)
US 4763180 A 19880809 (198834) 9p
EP 272476 B1 19930407 (199314) EN 15p
R: DE FR GB IT
DE 3785317 G 19930513 (199320)
ADT EP 272476 A EP 1987-117303 19871124; JP 63157463 A JP 1987-259877 19871016; US 4763180 A US 1986-945275 19861222; EP 272476 B1 EP 1987-117303 19871124; DE 3785317 G DE 1987-3785317 19871124, EP 1987-117303 19871124
FDT DE 3785317 G Based on EP 272476
PRAI US 1986-945275 19861222
AB EP 272476 A UPAB: 19930923
The semiconductor memory storage cell has a semiconductor substrate (10), and at least **two** laterally spaced vertical trenches in the substrate. The trenches are filled with doped **polysilicon** material (16). Conductive material (22,18,54,58) is disposed between each trench to form a conductive path between the doped **polysilicon** in each trench.

A layer (26,56) of epitaxial material is deposited over the substrate covering at least the conductive material (22,54) between the trenches. An insulator coated V-shaped groove provides a **gate** oxide which separates the conductive material between the trenches and the **polysilicon** filled trenches into separate storage capacitors. The doped layer region (30) on the epitaxial layer is separated into bit lines (BL).

ADVANTAGE - Array needs only single level of **polysilicon** and has no contacts.
1/14

L21 ANSWER 11 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1987-192327 [27] WPIX
DNN N1987-143991
TI Semiconductor **dynamic RAM memory** array - has
bit lines organised into **pairs** of adjacent poly **silicon**
lines coupled to memory cells in alternating configuration.
DC U14
IN KARP, J A
PA (VISI-N) VISIC INC
CYC 1
PI US 4675848 A 19870623 (198727)* 10p
ADT US 4675848 A US 1984-621848 19840618
PRAI US 1984-621848 19840618
AB US 4675848 A UPAB: 19930922
The **MOS dynamic random** access **memory**
(**DRAM**) device has an array of **dynamic RAM**
cells accessed by word and bit lines. Each memory cell comprises a single
field-effect transistor coupled by its source to the **gate** of an
MOS storage capacitor. The **word lines** are
coupled to their respective memory cells at the **gate** of the
field-effect transistor, while the bit lines are coupled to their
respective memory cells at the drain of the field-effect transistor.
The bit lines are organised into **pairs** of adjacent
polysilicon lines that are coupled to all the memory cells on both
sides of the bit lines in an alternating configuration. The **word**
lines are coupled to alternating **pairs** of cells on
opposite sides of the **word lines**.
ADVANTAGE - Allows 265K memory to fit into 16-pin plastic package.
3/14

L21 ANSWER 12 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1986-219932 [34] WPIX
CR 1989-326067 [45]
DNN N1986-164165
TI **DRAM** semiconductor memory cell with increased packing density -
has charge storing capacitor between channel of write transistor and
gate of read transistor.
DC U13 U14
IN MOCHIZUKI, T
PA (TOKE) TOSHIBA KK
CYC 5
PI EP 191435 A 19860820 (198634)* EN 38p
R: DE FR GB
JP 61222256 A 19861002 (198646)
JP 61184789 A 19860818 (198647)
JP 61227294 A 19861009 (198647)
JP 61227296 A 19861009 (198647)
US 4716548 A 19871229 (198802)
EP 191435 B 19900509 (199019)
R: DE FR GB
DE 3671124 G 19900613 (199025)
ADT EP 191435 A EP 1986-101610 19860207; JP 61222256 A JP 1985-64434 19850328;
JP 61184789 A JP 1985-25689 19850213; JP 61227294 A JP 1985-66809
19850330; JP 61227296 A JP 1985-67055 19850330; US 4716548 A US
1986-828863 19860212
PRAI JP 1985-25689 19850213; JP 1985-64434 19850328; JP 1985-66809
19850330; JP 1985-67055 19850330
AB EP 191435 A UPAB: 19931122

A **MOS** transistor (21), for writing data, has one terminal of it's drain-source path coupled to a bit line WB for writing data, and it's **gate** electrode connected to the **word line** (WW) for writing data. A second **MOS** transistor (22), for reading data, has one terminal of it's drain source path coupled to the bit line (RB) for reading data, and the other terminal of it's drain-source path coupled to the **word line** (RW) for reading data.

A capacitor (23) has one electrode connected to the other terminal of the drain-source path of the first **MOS** transistor and the other electrode connected to the **gate** of the second **MOS** transistor. Pref. the reading and writing bit lines (WB,RB) are common, or the reading bit line is shared by **two** memory cells. The transistors may be **polysilicon** on a substrate.
Dwg.4/23

L21 ANSWER 13 OF 25 WPIX (C) 2002 THOMSON DERWENT
AN 1985-291100 [47] WPIX
DNN N1985-217038
TI Metal insulated semiconductor **dynamic memory** with stacked capacitor - has polycrystalline **silicon** island-form conductive layers connected to diffusion regions and extending over **word lines**.
DC U13 U14
PA (FUIT) FUJITSU LTD
CYC 5
PI EP 161850 A 19851121 (198547)* EN 31p
R: DE FR GB
JP 60231357 A 19851116 (198601)
US 4754313 A 19880628 (198828)
EP 161850 B 19890726 (198930) EN
R: DE FR GB
DE 3571895 G 19890831 (198936)
ADT EP 161850 A EP 1985-302950 19850426; JP 60231357 A JP 1984-86635 19840428; US 4754313 A US 1987-93128 19870902
PRAI JP 1984-86635 19840428
AB EP 161850 A UPAB: 19930925

Two n+type diffusion regions (23,24) respectively provide, with a **gate** oxide layer (25), a transfer transistor (Tr). A respective **word line** is formed by a conductive layer (26) of n+ conductivity of polycrystalline **silicon** of thickness four to five thousand Angstroms which acts also as a **gate** electrode for the transfer transistor. An insulating film of **silicon** oxide (27) or nitride of thickness **two** thousand Angstroms covers each **word line**. One electrode of the capacitor is formed by a conductive layer (28) of polycrystalline **silicon** about **two** thousand Angstroms thick which is connected with the diffusion region. The dielectric of the capacitor is provided by a film (30) of **silicon** oxide or nitride. A further polycrystalline **silicon** layer (31) provides the other electrode of the capacitor.

An aluminium bit line (34) is in direct contact with an island layer (29) of conductive polycrystalline **silicon** at a contact window (33). The bit line contacts the diffusion region (24) indirectly.

ADVANTAGE - Highly-integrated memory construction is achieved which is less liable to short-circuits between bit lines and **word lines**.
5/11

L21 ANSWER 14 OF 25 JAPIO COPYRIGHT 2002 JPO

AN 1996-222706 JAPIO
TI SEMICONDUCTOR STORAGE DEVICE
IN YOSHIDA MASAKO; OWAKI YUKITO; HASEGAWA TAKEHIRO; OCHII KIYOBUMI; KOIZUMI MASAYUKI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 08222706 A 19960830 Heisei
AI JP1995-47550 (JP07047550 Heisei) 19950307
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 96, No. 8
AB PURPOSE: To make it possible to ensure the large signal traffic even if the cell capacity of a semiconductor storage device is decreased by a method wherein complementray data is written in a plurality of memory cells, which are linked to the same **word line** by each bit line **pair**, and one bit of data is stored in the plurality of memory cells.
CONSTITUTION: Memory cell arrays, which are respectively arranged with a **dynamic memory** cell, are respectively provided at the intersections of bit lines 16 and **word lines** 13 consisting of a first **polysilicon** layer. The **two** bit lines 16, which are arranged adjacent to each other or at intervals of a plurality of bit lines in the memory cell arrays, are paired to be used as a bit line **pair**. Complementary data is written in the **two** memory cells, which are linked to the same **word line** 13 by each of these bit line **pairs**, and one bit of data is stored in the **two** cells. Thereby, even if the cell capacity of a semiconductor storage device is decreased, the large signal traffic can be ensured, a noise margin is increased and the improvement of the reliability of the device can be contrived.

L21 ANSWER 15 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1995-141882 JAPIO
TI SEMICONDUCTOR MEMORY DEVICE
IN YAMADA TAKASHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 07141882 A 19950602 Heisei
AI JP1993-162757 (JP05162757 Heisei) 19930630
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 6
AB PURPOSE: To attain high-integration with a simple constitution by taking a **two** terminal element having a potential barrier as a wiring element and connecting one of electrodes of a capacitor with it and also connecting a reading **MOS** transistor with it.
CONSTITUTION: A **DRAM** is formed by arranging memory cells consisting of a writing element composed of the **two** terminal element having one potential barrier, a reading element composed of the **MOS** transistor and the capacitor for storing information in a matrix state on a (p) type **silicon** substrate 1. That is, an element separating insulation film 2 is formed on the substrate 1 and a memory cell is formed by arranging and forming 11 type diffusion layers 3a, 3b in the inside of the area. The capacitor is constituted of an electrode 9, an insulation film 4b and an electrode 5b and the electrode 5b becomes a **word line**. The **MOS** transistor as the reading element is constituted by making the electrode 5b operate also as the **gate** electrode of the **MOS** transistor and making an insulation film 4a to be a **gate** insulating film and by forming diffusion layers 3a, 3b becoming a source and a drain on the substrate 1.

L21 ANSWER 16 OF 25 JAPIO COPYRIGHT 2002 JPO

AN 1994-037256 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR DEVICE
IN SHIMABUKURO HIROSHI
PA FUJI ELECTRIC CO LTD, JP (CO 000523)
PI JP 06037256 A 19940210 Heisei
AI JP1992-187170 (JP04187170 Heisei) 19920715
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1548, Vol. 18, No. 255, P. 10 (19940516)
AB PURPOSE: To easily form a fin-type stacked capacitor by a method wherein **two** types of thin films alternately laminated are selectively etched, dielectric substance is buried, and opposed electrodes are formed.
CONSTITUTION: A field oxide film 2, a **word line** 3, interlayer insulating films 41 and 42, and a source region and a drain region both of N+-type, 51 and 52, are provided to a P-type **silicon** substrate 1, which is covered with a protective film 43, and PSG films 11 and LTO films 12 are alternately provided thereon. A through-hole 9 is formed by etching, only the PSG films 11 are etched as deep as prescribed, and a polycrystalline Si 60 is filled into produced empty spaces and patterned for the formation of fins 61, 62, and 63. The PSG films 11 and the LTO films 12 are removed at a time by etching, and the exposed surface of the polycrytsalline Si 60 is thermally oxidized to form a dielectric film 7 of SiO2. Cell plates 81, 82, and 83 serving as opposed electrodes and a joint 80 are formed and connected to a CP terminal, a **word line** 3 is connected to a WL terminal, and an N+ region 52 is connected to a BL terminal for the formation of a fin-type stacked capacitor of a **DRAM**.

L21 ANSWER 17 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1994-005815 JAPIO
TI SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
IN NISHIMURA MASAHIDE
PA FUJITSU LTD, JP (CO 000522)
PI JP 06005815 A 19940114 Heisei
AI JP1992-158371 (JP04158371 Heisei) 19920618
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1534, Vol. 18, No. 199, P. 138 (19940407)
AB PURPOSE: To reduce an element isolation part and to prevent a leakage of a junction by forming a plurality of opposite conductivity type diffused regions on a one conductivity type semiconductor substrate, wiring **two gates** between the adjacent regions, and forming a one conductivity type diffused region between the **two gates**.
CONSTITUTION: A thermal oxide SiO2 film 5 is formed as a **gate** insulating film on a p-- type Si substrate, 1 and **polysilicon** film **gates** (**word lines**) 6 are formed thereon. With photoresist 9 and the **gates** 6 as masks an impurity is ion implanted between the **two gates** 6 to form a p- type diffused region 4. Then, with photoresist 10 and the **gates** 6 as masks an impurity is ion implanted outside the **two gates** 6 to form n- type diffused regions 3. The ion implanted impurity is activated by heat-treating in a later step. According to such a configuration, an element isolation part can be contracted and leakage of a junction can be prevented. When it is applied to a **DRAM**, cells can be highly integrated.

L21 ANSWER 18 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1993-315568 JAPIO
TI SEMICONDUCTOR DEVICE
IN YOSHIDA NAOYUKI

PA NEC CORP, JP (CO 000423)
PI JP 05315568 A 19931126 Heisei
AI JP1992-143610 (JP04143610 Heisei) 19920508
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1516, Vol. 18, No. 12, P. 62 (19940225)
AB PURPOSE: To lessen the memory cell and the peripheral circuit of a **dynamic RAM** in level difference between them.
CONSTITUTION: A semiconductor device is provided with a stacked capacitor (8, 9, and 10), where a part of a **word line** located in an active region is formed of a **two**-layered film composed of a polycrystalline **silicon** film 4 and a tungsten silicide film 5 and the other part located on a field oxide film 2 is formed of only the polycrystalline **silicon** film 4.

L21 ANSWER 19 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1992-216667 JAPIO
TI SEMICONDUCTOR STORAGE DEVICE
IN NISHIHARA TOSHIYUKI
PA SONY CORP, JP (CO 000218)
PI JP 04216667 A 19920806 Heisei
AI JP1990-411136 (JP02411136 Heisei) 19901217
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1295, Vol. 16, No. 564, P. 124 (19921204)
AB PURPOSE: To facilitate the patterning of an upper layer (wiring or the like), enable the pattern layout with freedom, and increase the level of integration of a **DRAM** itself, by eliminating the formation and the increase of a step- difference following the formation of a stacked capacitor in a **DRAM**.
CONSTITUTION: The following are formed and a device is constituted; a switching element Tr1 constituted of a **word line** 4a and **two** source.cntdot.drain regions 5a, 5b, a switching element Tr2 constituted of a **word line** 4b and **two** source.cntdot.drain regions 5a, 5c, and a stacked capacitors C1 and C2 which are formed in the lower layers of Tr1 and Tr2, respectively, and constituted of the respective storage node electrodes 7a and 7b, a dielectric film 8, and a subplate electrode 9. In this case, the lamination technique of, e.g. **silicon** substrates applied to the formation of an SOI(**silicon** on insulator) substrate and the selective polishing technique for the **silicon** substrate can be used.

L21 ANSWER 20 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1986-269363 JAPIO
TI SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURE THEREOF
IN SOMATANI TOSHIFUMI; MIURA KENJI; NAKAJIMA BAN; MINEGISHI KAZUSHIGE; MORIE TAKASHI
PA NIPPON TELEGR & TELEPH CORP <NTT>, JP (CO 000422)
PI JP 61269363 A 19861128 Showa
AI JP1985-110128 (JP60110128 Showa) 19850524
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 500, Vol. 11, No. 122, P. 52 (19870416)
AB PURPOSE: To contrive the high velocity and the labor saving by reducing a **word line** load capacity by forming the first conductive layer to the depth in the middle of the groove formed on a main surface of the substrate of a semiconductor through an insulating film on the side plane of it and further forming the second conductor layer.
CONSTITUTION: In the one-transistor type **dynamic memory** cell, a transfer transistor 2 and a groove capacitor 3 are arranged in series along the side plane of the groove formed almost vertically to a

silicon substrate 1 and an isolation region 4 is arranged at the bottom of the groove. The first conductor 5 which functions as one electrode of a capacitor is formed through the insulating film 21 formed on the side plane of the groove. Also the second conductor layer 6 is formed in a predetermined region of the conductor 5, which functions as a **gate** electrode and a **word line**. On the region except this part, an insulating film is formed. Memory cells are located in the crossing region of bit lines 12 and the **word lines** 6 and a **gate** electrode 6 which is commonly used by **two** transfer transistors is limited to a region 13.

L21 ANSWER 21 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1986-082463 JAPIO
TI SEMICONDUCTOR MEMORY DEVICE
IN WATANABE SHIGEYOSHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 61082463 A 19860426 Showa
AI JP1984-204894 (JP59204894 Showa) 19840929
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 433, Vol. 1, No. 255, P. 87 (19860902)
AB PURPOSE: To microminiaturize a **D-RAM** memory cell while providing the reliability by storing writing charge at a conductor side, and using a substrate side as a plate, thereby preventing a leakage from a charge storage layer and a software error.
CONSTITUTION: **Two** memory cells made of a **MOS** transistor 12 and a **MOS** capacitor 13 are arranged on the element forming region 11 of the surface of an Si substrate 10. The transistor 12 uses a **word line** 14 mad of second **polysilicon** as a **gate** electrode, a drain side as a bit line 15 made of aluminum, and a source side as an electrode 21 connected through a P+ type diffused layer. The electrode 21 made of first **polysilicon** forms one electrode of the capacitor 13, the other electrode (plate electrode) is formed of the substrate 10, and the written charge is stored at the first **polysilicon** side. The electrode 21 is separated by an insulating film 25 and the substrate 10 from adjacent memory cell, and the leakage from the charge storage layer is extremely small.

L21 ANSWER 22 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1986-082462 JAPIO
TI SEMICONDUCTOR MEMORY DEVICE
IN WATANABE SHIGEYOSHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 61082462 A 19860426 Showa
AI JP1984-204887 (JP59204887 Showa) 19840929
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 433, Vol. 1, No. 255, P. 87 (19860902)
AB PURPOSE: To microminiaturize a **D-RAM** memory cell while proving the reliability by storing writing charge at a conductor side, and using a substrate side as a plate, thereby preventing a leakage from a charge storage layer and a software error.
CONSTITUTION: **Two** memory cells made of a **MOS** transistor 12 and a **MOS** capacitor 13 are arranged on the insulator region 11 of the surface of an Si substrate 10. The transistor 12 uses a **word line** 14 mad of second **polysilicon** as a **gate** electrode, a drain side as a bit line 15 made of aluminum, and a source side as an electrode 21 connected through a P+ type diffused layer. The electrode 21 made of first **polysilicon** forms one electrode of the capacitor 13, the other electrode (plate electrode) is formed of the substrate 10, and the written

charge is stored at the first **polysilicon** side. The capacitor 13 is separated by a thick insulating film 27 from the adjacent memory cell, and the leakage from the charge storage layer is extremely small.

L21 ANSWER 23 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1985-196967 JAPIO
TI **DYNAMIC MEMORY** CELL
IN NAKAMURA TADASHI; AKAOGI TOSHIO; TAKEISHI TSUGUKAZU
PA TOPPAN PRINTING CO LTD, JP (CO 000319)
PI JP 60196967 A 19851005 Showa
AI JP1984-53745 (JP59053745 Showa) 19840321
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 381, Vol. 1, No. 39, P. 164 (19860215)
AB PURPOSE: To short-circuit signal retardation time in a **word line** and a bit line by forming the **word line** and the bit line by **double** layer Al wirings.
CONSTITUTION: N+ layers 22 are brought into contact with N layers 26 for a connection to a capacitor. A first **polysilicon** layer 30 is formed on a P- substrate 20 shaped by N and N+ layers 26, 22, 24 through an insulator layer 28 consisting of SiO2, etc. The layer 30 is formed to the upper section of the N layer 26 so as to function as an electrode for a capacitor, and a window-shaped opening section is formed to the first **polysilicon** layer 30 corresponding to a forming region for an MOSFET. Second **polysilicon** layers 32 are shaped on the substrates 20 among the N+ layers 22 and the N+ layers 24, and used as **gates** for the MOSFET. Since a **word line** and a bit line are formed by aluminum layers, a **dynamic RAM**, in which signals are hardly retarded by the **word line** and the bit line and which can be operated at high speed, is realized.

L21 ANSWER 24 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1983-204568 JAPIO
TI SEMICONDUCTOR DEVICE
IN HAGIWARA TAKAAKI; ASAI SHOJIRO; MIYAO MASANOBU
PA HITACHI LTD, JP (CO 000510)
PI JP 58204568 A 19831129 Showa
AI JP1982-86627 (JP57086627 Showa) 19820524
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 230, Vol. 8, No. 491, P. 138 (19840306)
AB PURPOSE: To highly integrate a semiconductor device by simultaneously forming elements on not only one surface of a semiconductor but more than **two** surfaces including back and side surfaces.
CONSTITUTION: An SiO2 film 7 is formed on an Si substrate 1, a thin film 2 of single crystal of almost single crystal is formed, and an SiO2 film 4 and a **polysilicon gate** 3 are formed. Diffused layers 6, 6' are formed on the film 2, the **gate** 3 is used as a **word line**, and the layer 6 is used as a bit line. The formation of the diffused layer is prevented on the side faces of the thin film 2 at the bit line side 6, and the layer 6' is formed on the side face of opposite side. When the voltage for inverting the polarity of the film 2 is applied to the substrate 1, a node (diffused layer 6') at opposite side to the bit line of a switching element is connected to the back surface 8 of the thin film. Accordingly, the capacity between the back surface 8 and the substrate 1 can be used as the capacity of **dynamic RAM**, thereby remarkably reducing the area. It is effective to provide a diffused layer 9 due to the reduction in the resistance of the substrate 1. According to this configuration, a **dynamic RAM** of high integration is completed in which the switch element is arranged on the front surface and a capacitive

element is arranged on the back surface.

L21 ANSWER 25 OF 25 JAPIO COPYRIGHT 2002 JPO
AN 1981-029362 JAPIO
TI SEMICONDUCTOR **DYNAMIC MEMORY**
IN TANAKA SHOICHI
PA TANAKA SHOICHI, JP (IN)
PI JP 56029362 A 19810324 Showa
AI JP1979-106215 (JP54106215 Showa) 19790820
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 59, Vol. 5, No. 821, P. 48 (19810529)
AB PURPOSE: To obtain a high integrity memory device by a **VMOS** technique by forming an N type memory region on a P- type epitaxial layer on a P+ type Si substrate by self-diffusion with its density of P+>N>P-. CONSTITUTION: B is selectively added to a P+ type Si substrate added with P and a plane <100>, and a P- type epitaxial layer 3 is laminated thereon. At this time a thin N type memory region 2 is formed owing to the difference of rediffusion of the P and the B. Then, an N+ type bit region 4 is formed on the upper portion of the region 2, an SiO2 film 5 is coated thereon, an opening is perforated at the film 5, is anisotripically etched to form a V-shaped groove 6 to divide the regions 4 and 2 into **two**. Since the layer 2 is thin and has no punch-through therebetween, the V- shaped groove may be reduced to improve the integrity. Subsequently, an SiO2 film 7 is coated on the oblique surfaces of the groove, and a **polysilicon word line** 8 is formed thereon. The junction capacity between the N type layer 2 and the P+ type substrate stores charge, so that the oblique surfaces of the groove under the work line 8 becomes the N type channel of the VMOST. This configuration can obtain a high integrity and preferable area efficiency in memory cell.

L23 ANSWER 1 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 2002-291221 [33] WPIX
DNN N2002-227374 DNC C2002-085369
TI Semiconductor device has transfer **gates**, contact plugs, first and second interlayer insulating films, and diameter-reduced contact plugs.
DC L03 U11 U12 U13
IN SHINKAWATA, H
PA (MITQ) MITSUBISHI ELECTRIC CORP; (MITQ) MITSUBISHI DENKI KK
CYC 2
PI US 2002008324 A1 20020124 (200233)* 28p
JP 2002043544 A 20020208 (200233) 20p
ADT US 2002008324 A1 US 2001-766846 20010123; JP 2002043544 A JP 2000-220609 20000721
PRAI JP 2000-220609 20000721
AB US2002008324 A UPAB: 20020524

NOVELTY - A semiconductor device comprises: transfer **gates**; contact plugs adjacent to the transfer **gates**; a first interlayer insulating film; a second interlayer insulating film formed on the first insulating film; and diameter-reduced contact plugs which are smaller than the contact plugs and extend through the second insulating film to conduct to the contact plugs, respectively.

DETAILED DESCRIPTION - A semiconductor device comprises: transfer **gates** (33); contact plugs (50, 68) adjacent to the transfer **gates**; a first interlayer insulating film; a second interlayer insulating film formed on the first interlayer insulating film; and diameter-reduced contact plugs which are smaller than the contact plugs and extend through the second interlayer insulating film to conduct to the contact plugs, respectively. Each transfer **gate** has a **gate** insulating film, a **gate** electrode layer, and side walls for covering sides of the **gate** insulating film and the **gate** electrode layer. Each contact plug has the same height as the transfer **gate** and is adjacent to the transfer **gate** over the whole height. The first interlayer insulating film has a surface that defines the same surface as that of the transfer **gate** and the contact plug.

An INDEPENDENT CLAIM is also included for a method of manufacturing the semiconductor device, comprising: depositing the first insulating film on a **silicon** substrate; forming the transfer **gate** holding trenches in the first insulating film; forming side walls of each transfer **gate** in the transfer **gate** holding trenches; forming a **gate** insulating film and a **gate** electrode layer of each transfer **gate** within a space interposed between the side walls; etching portions adjacent to the transfer **gates**, of the first insulating film under a condition that the first insulating film is capable of being removed at a high selectivity with respect to a material which constitutes each transfer **gate**, thus forming contact holes adjacent to the transfer **gates** in a self-aligned manner; forming the contact plugs in the contact holes, respectively; forming the second insulating film on the first insulating film, the contact plugs and the transfer **gates**; forming the diameter-reduced contact holes which are smaller than the contact plugs and in communication with the contact plugs, in the second insulating film; and forming the diameter-reduced contact plugs which conduct to the contact plugs, in the diameter-reduced contact holes.

USE - Semiconductor memory device.

ADVANTAGE - The semiconductor device has a structure suitable for the

reliable formation of a miniaturized **dynamic random** access **memory**.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of a semiconductor device.

Transfer **gates** 33
Contact plugs 50, 68
Bit line 60
Capacitor contact plugs 64
Lower electrodes 72
Barrier metal 96
Dwg.14A/30

L23 ANSWER 2 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 2001-637641 [73] WPIX
DNN N2001-476475
TI Fabrication method for **dynamic random** access **memory**, involves forming source and drain regions which are having separated light and heavily doped regions using **double** spacers.
DC U11 U13 U14
IN LEE, R
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 6214677 B1 20010410 (200173)* 8p
ADT US 6214677 B1 US 1999-426923 19991022
PRAI US 1999-426923 19991022
AB US 6214677 B UPAB: 20011211

NOVELTY - The source region (114) having separate lightly and heavily doped regions (110,113) is formed on the substrate by having **silicon** oxide layer (112) as mask. The drain regions (136,137) having separate light and heavily doped regions are formed on the substrate by having tungsten spacer (120) as mask.

DETAILED DESCRIPTION - A pad oxide layer (104) with opening (108) and a **silicon** nitride layer (106) are formed subsequently on the substrate (100) with insulating structure (102). A lightly doped region (110) is formed in the substrate. By having the **silicon** oxide layer (112) as spacer, a heavily doped region (113) is formed by ion implementation. The regions (110,113) which do not overlap with each other forms the source region (114). A **polysilicon bit line** (116) coupled to source region, fills the opening (108). The layers (104,106) are removed and a **gate** oxide layer (118) is formed on the exposed substrate. A tungsten spacer (120) is formed to cover the side wall of the layer (112). By having the spacer (120) as hard mask, a lightly doped drain region (122) is formed. An oxide layer is formed to cover the layers (118,116,112). The oxide layer spacers and layer (116) are polarized to form a planarized oxide layer (124). A dielectric layer (126) having contact opening (128) is formed on the substrate. A **polysilicon** layer (130) filling the contact opening is coupled with **bit line**. An inter **polysilicon** dielectric (IPD) layer is formed on conductive layer (130). Lightly doped drain region (122) and heavily doped drain region are formed to form drain region (136). A **polysilicon** electrode fills the storage node opening (134) on the IPD layer.

USE - For fabricating semiconductor devices especially **metal oxide semiconductor dynamic random** access **memory** (**MOS-DRAM**) capacitor.

ADVANTAGE - Reduces the channel length between source and drain region. Hence the size and area occupied by the **DRAM** capacitor are reduced without reducing capacitor range.

DESCRIPTION OF DRAWING(S) - The figure shows the schematic cross

sectional diagrams for **DRAM** fabrication.
Substrate 100
Insulating structure 102
Pad oxide layer 104
Silicon nitride layer 106
Opening 108,134
Lightly and heavily doped source regions 110,113
Silicon oxide layer 112
Source region 114
Polysilicon bit line 116
Gate oxide layer 118
Tungsten spacer 120
Doped drain regions 122
Planarized oxide layer 124
Dielectric layer 126
Contact opening 128
Polysilicon layer 130
Drain regions 136,137
1B, 1C, 1G/1

L23 ANSWER 3 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1997-086043 [08] WPIX
DNN N1997-070912 DNC C1997-027951
TI Fabricating **dynamic random** access **memory** with **E**-shaped capacitor - including planarising dielectric and poly **silicon** by chemical mechanical polishing.
DC L03 U11 U13
IN LIANG, M; WANG, C
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO LTD
CYC 1
PI TW 288164 A 19961011 (199708)* 15p
ADT TW 288164 A TW 1996-100421 19960115
PRAI TW 1996-100421 19960115
AB TW 288164 A UPAB: 19970220
A method of fabricating **dynamic random** access **memory** (**DRAM**) comprises: (1) forming active area and field oxide on semiconductor substrate; (2) forming **metal oxide semiconductor** field effect transistor (MOSFET) containing **gate** oxide, **gate** electrode, spacer and source/drain; (3) depositing first dielectric and etching the above first dielectric to form **bit line** contact; (4) forming **bit line**; (5) depositing second dielectric and third dielectric to overlay the above **bit line**, and by chemical mechanical polishing planarising the above third dielectric; (6) by lithography and etch technique on capacitor region etching the above first dielectric, second dielectric and third dielectric to form node contact, and subsequent capacitor storage node electrically contacts with MOSFET through the above node contact; (7) depositing one first **polysilicon** to fill the above node contact and contact with source; (8) by chemical mechanical polishing performing polishing treatment to the above first **polysilicon** and third dielectric, in which the above polishing treatment removes one portion of the above third dielectric and reserves **polysilicon** pillar in node contact; (9) by lithography and etch technique on capacitor region etching the above third dielectric of some thickness on **two** sides of the above **polysilicon** pillar, so as to form trench on **two** sides of the above **polysilicon** pillar; (10) depositing one second **polysilicon** which does not fill the above trench; (11) depositing fourth dielectric which fill the above trench; (12) by chemical

mechanical polishing performing polishing treatment to the above fourth dielectric, second **polysilicon** and third dielectric and stop below top surface of the above **polysilicon** pillar; (13) removing left portion of the above third dielectric and fourth dielectric, and the above left **polysilicon** pillar and second **polysilicon** constitute capacitor storage node; and (14) forming one very thin capacitor dielectric on the above storage node surface, then forming one third **polysilicon**, and by lithography and etch technique etching the above capacitor dielectric and third **polysilicon** to form capacitor top electrode.
Dwg.10/10

L23 ANSWER 4 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1995-134798 [18] WPIX
CR 1994-162040 [20]; 1994-179842 [22]; 1994-288953 [36]
DNN N1998-182969 DNC C1998-072288
TI **Dynamic random** access **memory** - has trench formed in substrate with conductive storage layer partly covered by island-shaped insulating layer, and source or drain of transistor attached to trench.
DC L03 M21 P51 P52 U11 U12 U13 U14 U21
IN AOKI, M; HAMAMOTO, T; HIEDA, K
PA (TOKE) TOSHIBA KK; (TOKE) TOSHIBA CORP
CYC 3

PI	JP 07058217	A	19950303	(199518)*	8p
	US 5508541	A	19960416	(199621)	56p
	US 5736760	A	19980407	(199821)B	55p
	KR 139834	B1	19980817	(200021)	

ADT JP 07058217 A JP 1993-201554 19930813; US 5508541 A US 1993-124300 19930920; US 5736760 A Div ex US 1993-124300 19930920, US 1996-632321 19960415; KR 139834 B1 KR 1993-19255 19930922
FDT US 5508541 A JP 06104399, JP 06120450, JP 06126335; US 5736760 A Div ex US 5508541
PRAI JP 1993-201554 19930813; JP 1992-278110 19920922; JP 1992-286684 19920930; JP 1993-3931 19930113
AB US 5736760 A UPAB: 19980528 ABEQ treated as Basic
The semiconductor memory cell includes a semiconductor substrate with **two** well regions which are superposed on each other. A trench (56) extends past the first well region (54) into the second well region. The well regions have different conductivities. A capacitor has a storage node and an insulated layer buried in the trench. The storage node has a **double**-layered structure. An island-shaped layer (68) covers the upper surface of the storage node portion on the substrate. The island-shaped layer is coupled to the storage node on the substrate. The upper surface of the island-shaped layer is set in the same level in position as an upper surface of the substrate.

A transistor with a source and a drain defines a channel region between them in the substrate. An insulated **gate** overlies the channel region and extends over the island-shaped layer. Either the source or the drain is positioned next to the trench and is coupled to the island-shaped layer. The other is connected directly to a corresponding data-transfer line. The source and drain are formed in the first well region. A dielectric layer is arranged inside and around the trench in the substrate. The dielectric layer is deeper than the first well region and shallower than the trench.

USE - Also for NAND type **DRAM**.

ADVANTAGE - Increases reliability by maintaining cut-off characteristic of **MOS** transistor. Reduces junction leak.
Dwg.34B/57

AB JP 07058217 A UPAB: 20000502
The semiconductor memory is formed on P type **silicon** substrate (1). P type epitaxial layer (2) is formed on the **silicon** substrate. Trenches (4) are formed in the epitaxial layer extending to the **silicon** substrate. The storage electrode (6) is formed in these trenches. A capacitor insulating film separates the trench electrode and the trench inner walls.

Epitaxial **silicon** layer (40) is formed in contact with P type epitaxial layer. Interlayer insulating film (12) is formed on epitaxial Si layer. **Bit line** (13) is formed on the surface of interlayer insulating film.

ADVANTAGE - Secures alignment margin of trench capacitor and element region. Realizes miniaturized memory cell with stable operation.
Dwg.2/12

L23 ANSWER 5 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1995-068198 [10] WPIX
DNN N1995-054162
TI SOI semiconductor device e.g. for solid state memory - has **MOS** devices formed on isolation layer with further isolation layers overlaid and with **bit line** connections.
DC U13 U14
IN OASHI, T
PA (MITQ) MITSUBISHI DENKI KK; (MITQ) MITSUBISHI ELECTRIC CORP
CYC 3
PI
DE 4421633	A1	19950202	(199510)*	41p
JP 07022517	A	19950124	(199513)	18p
US 5406102	A	19950411	(199520)	40p
DE 4421633	C2	20010222	(200111)	

ADT DE 4421633 A1 DE 1994-4421633 19940621; JP 07022517 A JP 1993-150231 19930622; US 5406102 A US 1994-253019 19940602; DE 4421633 C2 DE 1994-4421633 19940621
PRAI JP 1993-150231 19930622
AB DE 4421633 A UPAB: 19950314
The solid state memory is configured as a so called SOI-MOSFET device in which an isolation layer (13) is formed on a **silicon** substrate (11). Onto this formed a number of **silicon** layers (1) in a matrix arrangement as islands, with spaces filled by **silicon** nitride (15a).

The **silicon** layers are coupled to **bit lines**. **MOS** transistors (10) are formed with **gate** electrodes (3), source/drain regions (7) and insulation (5). Further isolation layers (19, 20) are formed around the cells and an electrode layer (25) is formed on a buffer insulation layer (31).

ADVANTAGE - Reduced isolation layers.
Dwg.2/36

L23 ANSWER 6 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1989-078245 [11] WPIX
DNN N1989-059778
TI Sense amplifier structure for read-out **DRAM** integrated circuit - has **pair** of conductivity cross-coupled field effect transistor connected between **pair** of nodes and latching device.
DC U14
IN DHONG, S H; LU, N C C; LU, N C
PA (IBMC) IBM CORP; (IBMC) INT BUSINESS MACHINES CORP
CYC 4
PI EP 306712 A 19890315 (198911)* EN 13p
R: DE FR GB

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     US 4816706     A   19890328 (198915)        12p
     EP 306712      B1 19931229 (199401)   EN    15p
         R: DE FR GB
     DE 3886632     G   19940210 (199407)
ADT  EP 306712 A EP 1988-112792 19880805; US 4816706 A US 1987-95061 19870910;
     EP 306712 B1 EP 1988-112792 19880805; DE 3886632 G DE 1988-3886632
     19880805, EP 1988-112792 19880805
FDT  DE 3886632 G Based on EP 306712
PRAI US 1987-95061     19870910
AB   EP    306712 A UPAB: 19930923
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The amplifier has a latching device (22) connected to a source of supply voltage (VDD). A **pair** of conductivity type cross-coupled field-effect transistors (14,10) connect together between first and second nodes of at least one **pair** of connecting nodes and the latching device. A second latching device (24) is connected to ground potential. A second **pair** of conductivity cross-coupled field-effect transistor (18,20) are connected together between first and second nodes of a **pair** of connecting nodes and a second latching device.

A first **bit line** (26) and second complementary **bit line** (28) conducts biline signals of varying **bit line** voltage magnitudes. A voltage limiting device is connected to at least one **pair** of connecting nodes for limiting the magnitudes of **bit line** voltage.

USE/ADVANTAGE - Complementary metal-oxide-**silicon** field effect transistor. (CMOS-FET) sense amplifiers for readout of **dynamic random** access **memory** (**DRAM**) integrated circuit structures. Improved sensing speed without increased power consumption and insymmetrical **bit line** voltage swing.

1/10

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L23  ANSWER 7 OF 13  WPIX (C) 2002 THOMSON DERWENT
AN   1987-137439 [20]   WPIX
DNN  N1987-103007
TI   FET sense amplifier - comprises flip-flop elements with same source drain
     alignments in self-aligned process.
DC   U13 U14
IN   NOGAMI, K
PA   (TOKE) TOSHIBA KK
CYC  5
PI   EP 222396      A   19870520 (198720)* EN    19p
         R: DE FR GB
     JP 62115861    A   19870527 (198727)
     EP 222396      B   19910123 (199104)
         R: DE FR GB
     DE 3677141     G   19910228 (199110)
     US 5175604     A   19921229 (199303)         9p
ADT  EP 222396 A EP 1986-115726 19861112; US 5175604 A Cont of US 1986-929359
     19861112, US 1991-681665 19910408
PRAI JP 1985-256084    19851115
AB   EP    222396 A UPAB: 19930922
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The field-effect transistor device comprises a semiconductor substrate (54) and a number of FETs (Q1,Q2,Q3,Q4) each having a **gate** electrode formed over the semiconductor substrate. Source and drain regions are self-aligned in the semiconductor substrate on **two** opposing sides of the **gate** electrode, respectively and a wiring device connects the FET's.

The source-to-drain paths of the FETs are oriented in a number of conductor layers for combining the FET's as a sense amplifier.

ADVANTAGE - Transistors have some drive capability and enhance speed and sensitivity of sense amplifier.
5/6

L23 ANSWER 8 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1985-231488 [38] WPIX
DNN N1985-173454 DNC C1985-100406
TI Semiconductor memory device - has poly **silicon** electrodes formed over substrate recess portions.
DC L03 U11 U13 U14
IN MASUOKA, F
PA (TOKE) TOSHIBA KK
CYC 3
PI EP 154685 A 19850918 (198538)* EN 35p
R: DE FR GB
EP 154685 B 19900418 (199016)
R: DE FR GB
ADT EP 154685 A EP 1984-114160 19810121
PRAI JP 1980-7524 19800125; JP 1980-7519 19800125; JP 1980-7520 19800125
AB EP 154685 A UPAB: 19970909
Memory device comprises: a substrate having a recess; a polySi electrode insulatively disposed over the recess, with at least one capacitor formed between substrate and electrode; and a **MOS** transistor formed on at least one side of the poly electrode.
Pref. further recess(es) are formed in the polyelectrode in correspondence with the substrate recess(es).
ADVANTAGE - Recess arrangement permits stepped portions of multilayered wirings to be eliminated and capacitance due to digit lines to be decreased.
Dwg.4/24

L23 ANSWER 9 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1981-F4129D [24] WPIX
TI **MOS** matrix read and write memory - uses split matrix of **MOS** dynamic cells with serial input and output of data.
DC U14
IN RAO, G R M; REDWINE, D J; WHITE, L S
PA (TEXI) TEXAS INSTR INC
CYC 2
PI DE 3032298 A 19810604 (198124)*
US 4321695 A 19820323 (198214)
US 4330852 A 19820518 (198222)
US 4347587 A 19820831 (198237)
DE 3032298 C 19911219 (199151)
PRAI US 1979-97104 19791123; US 1979-97105 19791123; US 1979-97106 19791123
AB DE 3032298 A UPAB: 19930915
The read-write matrix memory is based upon **dynamic MOS memory** cells and has facility for serial data access. The memory has a total of 65,536 cells arranged in a single **dual**-in-line 16 pin integrated circuit. The memory cells are arranged in **two** sections, each with 32,768 cells to give a total matrix of 256 lines and 256 columns. The 8 **bit line** address is transmitted to **two** halt line capacity decoders.
Serial data input is multiplexed into **two** serial shift registers and data output is handled by the same register stages. The memory access process is controlled by an on chip clock signal generator.

L23 ANSWER 10 OF 13 WPIX (C) 2002 THOMSON DERWENT
AN 1980-D4132C [15] WPIX
TI **Dynamic random** access **memory** - has polycrystalline **silicon bit lines** formed on monocrystalline **silicon** chip and contacting only sources of MOSFETs.
DC U14
IN CLEMENS, J T; CUTHBERT, J D; PROCYK, F J
PA (AMTT) WESTERN ELECTRIC CO INC
CYC 6
PI WO 8000641 A 19800403 (198015)* EN
RW: FR
W: DE GB JP NL
NL 7920087 A 19800731 (198033)
GB 2043999 A 19801008 (198041)
US 4240195 A 19801222 (198102)
EP 20477 A 19810107 (198103) EN
R: FR
DE 2953111 A 19801127 (198129)
JP 55500649 A 19800911 (198148)
EP 20477 B 19840808 (198432) EN
R: FR
PRAI US 1978-942861 19780915
AB WO 8000641 A UPAB: 19940205
The **dynamic random** access **memory** has memory cells arranged in a 2-D array of rows and columns in a **silicon** chip. The chip includes active portions each having a **pair** of **two** adjacent cells in respective common columns.
A set of conductors (47A) interconnects all the storage electrodes and separate conductors of a second set interconnect all the **gate** electrodes in a common row. Separate conductors (50) of a third set (50) is a polycrystalline silicone line overlying the chip and making direct electrical contact with source zones (41) but otherwise insulated from the chip.

L23 ANSWER 11 OF 13 JAPIO COPYRIGHT 2002 JPO
AN 1992-274359 JAPIO
TI **DYNAMIC RANDOM** ACESS **MEMORY**
IN YANAGI MASAHIKO
PA SHARP CORP, JP (CO 000504)
PI JP 04274359 A 19920930 Heisei
AI JP1991-34870 (JP03034870 Heisei) 19910301
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1319, Vol. 17, No. 71, P. 66 (19930212)
AB PURPOSE: To increase the ratio of the area of a capacitor to the area of a cell further by forming the capacitor between a transistor formed onto a substrate and a thin-film transistor in a **dynamic random** access **memory**.
CONSTITUTION: The information of **two** bits is stored by **two** access transostors 4, 5 and one capacitor 8 in the **dynamic random** access **memory**. The capacitor 8 is formed to the upper section of the first access transistor 4 shaped onto a **silicon** substrate 20 or the second access transistor 5 composed of a thin-film transistor to the upper section of the capacitor 8 at that time. Accordingly, three-dimensional structure in which the substrate transistor 4, the capacitor 8 and the thin-film transistor 5 are superposed is formed, thus reducing contact holes, etc., with a **bit line** 2 and structure in which the area of the capacitor 8 is lost.

L23 ANSWER 12 OF 13 JAPIO COPYRIGHT 2002 JPO
AN 1990-079462 JAPIO
TI SEMICONDUCTOR MEMORY
IN YAMADA TAKASHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 02079462 A 19900320 Heisei
AI JP1988-230955 (JP63230955 Heisei) 19880914
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 937, Vol. 14, No. 259, P. 71 (19900605)
AB PURPOSE: To provide a **DRAM** in laminate type capacitor and cell construction, which gives a sufficient capacitance with good reliability using minor occupation area, by interposing a pad electrode between a **bit line** and a diffusion layer in connection therewith, stretching partially this pad electrode to the overlapped portion of the **gate** electrode of a **MOS** transistor with the lower electrode of capacitor, and arranging so as to be pinched by this **gate** electrode and lower electrode.
CONSTITUTION: With a **gate** insulation film 4 interposed, a **gate** electrode 5 is formed in a region bounded by an element separate insulation film 2 of a P-type **silicon** substrate 1, and on this electrode 5 n-type diffusion layers 61, 62 are formed, which become a source and a drain diffusion layer selfaligningly, to constitute a **MOS** transistor. As basis to a **bit line** a pad electrode 8 is formed in this diffusion layer 61, with which the **bit line** is in contact, in such an arrangement as partially enclosing the **gate** electrode 5. Pattern of the lower electrode 10 of capacitor is so formed as stretching to over the **gate** electrode 5 and pad electrode 8 while getting over the level difference in the laminate structure of these **two**. Thus, a large capacitance is accomplished by minor occupation area.

L23 ANSWER 13 OF 13 JAPIO COPYRIGHT 2002 JPO
AN 1989-025463 JAPIO
TI SEMICONDUCTOR MEMORY CELL
IN IWATA YOSHIYUKI; FUKUMOTO MASANORI; YASUHIRA MITSUO; YABU TOSHIKI; ICHIKAWA YOHEI; MATSUYAMA KAZUHIRO; OSONE TAKASHI
PA MATSUSHITA ELECTRIC IND CO LTD, JP (CO 000582)
PI JP 01025463 A 19890127 Heisei
AI JP1987-181473 (JP62181473 Heisei) 19870721
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 759, Vol. 13, No. 213, P. 38 (19890518)
AB PURPOSE: To perform a semiconductor memory cell which can cope with a large capacity and high density **DRAM** by forming all charge storage capacitor, a field effect transistor and an element isolating region in a trench.
CONSTITUTION: A trench is so formed on a P-type Si substrate 1 that a memory cell remains insularly, a P+ type diffused layer region 5 is formed in the bottom of the trench to isolate elements between adjacent memory cells. A charge storage capacitor is composed of a storage electrode 2 of an N+ type diffused layer region, a capacitor oxide film 3, and a **polysilicon** plate electrode 4. Numeral 7 denotes an N+ type diffused layer region, numeral 8 denotes a **polysilicon** film, numeral 9 denotes an SiO2 film, numeral 2 is a source, numeral 7 is a drain, numeral 8 is a **gate**, and numeral 9 is a **gate** oxide film. Thus, a vertical **MOS** transistor is formed on the top of the sidewall of the trench, and **two MOS** transistors are provided in one memory cell. A **bit line** 12 is connected through a contact region 13 to the drain 7.

L30 ANSWER 1 OF 1 WPIX (C) 2002 THOMSON DERWENT
AN 1990-046091 [07] WPIX
DNN N1990-035389 DNC C1990-020029
TI CMOS one-capacitor DRAM - uses non-boosted **word line** without suffering threshold loss.
DC L03 U13 U14
IN DHONG, S H; HENKELS, W H; LU, N C C; LU, N C
PA (IBMC) INT BUSINESS MACHINES CORP; (IBMC) IBM CORP
CYC 14
PI EP 354348 A 19900214 (199007)* EN 9p
R: CH DE ES FR GB IT LI NL SE
JP 02068792 A 19900308 (199016)
US 4910709 A 19900320 (199017)
US 4927779 A 19900522 (199024)
CN 1040462 A 19900314 (199050)
CA 1314991 C 19930323 (199317)
KR 9211046 B1 19921226 (199415)
ADT EP 354348 A EP 1989-112325 19890706; JP 02068792 A JP 1989-184889 19890719; US 4910709 A US 1988-230410 19880810; US 4927779 A US 1989-428159 19891027; CA 1314991 C CA 1989-600744 19890525; KR 9211046 B1 KR 1989-9780 19890710
PRAI US 1988-230410 19880810
AB EP 354348 A UPAB: 19930928
A memory cell structure (8) for a dynamic semiconductor array, operating with a non-boosted **wordline** and without a threshold loss problem, and having pairs of **wordlines** (26, 28) for transmitting signals, each at two signal levels, comprises an MNOS (18) and a PMOS (12) device, both including first and second gate electrodes, and a storage capacitor (30). The first electrodes of the transistors are connected to a **bit line** (34) of the memory array, and the second electrodes to the capacitor (30). The NMOS and CMOS gate electrodes (18, 20) are connected to the first and second **wordlines** (26, 28) respectively, and the transistors are turned off by the first signal level on the **wordlines** and on at the second signal level. The **bit line** is connected to the capacitor, charge being stored into and read out from the capacitor in response to the turning on and off of the transistors.

USE/ADVANTAGE - A CMOS one-capacitor DRAM and method of fabrication are provided, the cell operating with a non-boosted **wordline** but without suffering from the threshold loss problem. Thus the area of the DRAM cells may be reduced.
1/5

L31 ANSWER 1 OF 8 WPIX (C) 2002 THOMSON DERWENT
AN 2001-501683 [55] WPIX
CR 2001-315686 [32]
DNN N2001-371997
TI Trench capacitor type **DRAM** cell has vertical **metal oxide semiconductor** field effect transistor transfer device in upper portion of deep trenches and collar isolation oxide in upper portion on deep trench side walls.
DC U13 U14
IN FURUKAWA, T; HAKEY, M C; HORAK, D V; MA, W H; MANDELMAN, J A
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 1
PI US 6184549 B1 20010206 (200155)* 10p
ADT US 6184549 B1 Div ex US 1998-86057 19980528, US 1999-296807 19990423
PRAI US 1998-86057 19980528; US 1999-296807 19990423
AB US 6184549 B UPAB: 20010927

NOVELTY - Deep trenches (74,75,74',75') are formed in p type substrate with lower portion partially filled with n+ **polysilicon** storage node and surrounded by n+ **silicon** storage plate. Vertical MOSFET transfer device is formed in upper portion of trenches. A collar isolation oxide is formed in upper portion on deep trench side walls between n+ buried strap diffusion of MOSFET and storage plate.

DETAILED DESCRIPTION - A recessed **polysilicon** conductor is provided within upper portion of deep trenches gating and p type **silicon** adjacent deep trench. A gate conductor connects an n+ **bit line** diffusion (65) formed above p type **silicon** and n+ buried strap diffusion. Several recessed active and passive **wordline** conductors are formed on insulating layer above trenches.

USE - Trench capacitor type integrated circuit dynamic random access memory.

ADVANTAGE - Byintegrating robust transfer device in dynamic random access memory cell with shallow trench isolation region constructed between adjacent trench capacitor cells, the device channel length requirement is made independent of cell size, thus the dimension of device can be reduced. Using square printing to form shallow trench isolation and detrenches, scaling of the cell to very small dimensions is allowed.

DESCRIPTION OF DRAWING(S) - The figure shows the cross sectional view of trench capacitor type DRAM cell.

Line diffusion 65
Deep trenches 74,75,74',75'

Dwg.9/11

L31 ANSWER 2 OF 8 WPIX (C) 2002 THOMSON DERWENT
AN 1999-347086 [29] WPIX
DNN N1999-259535 DNC C1999-102042
TI Three device bipolar complementary metal oxide semiconductor (BICMOS) gain cell for a dynamic read only memory (DRAM).
DC L03 U13 U14
IN BERTIN, C L; FIFIELD, J A; HOUGHTON, R J; MILLER, C P; TONTI, W R
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 2
PI US 5909400 A 19990601 (199929)* 12p
KR 99023762 A 19990325 (200024)
KR 299344 B 20011019 (200234)
ADT US 5909400 A US 1997-917630 19970822; KR 99023762 A KR 1998-33929 19980821; KR 299344 B KR 1998-33929 19980821
FDT KR 299344 B Previous Publ. KR 99023762

PRAI US 1997-917630 19970822
AB US 5909400 A UPAB: 19990723
NOVELTY - The storage capacitor is connected between the storage node and the substrate of the gain cell, and the collector of the PNP transistor is also connected to the substrate. During a read operation the previously precharged capacitive read **bit line** is rapidly discharged through the series connected read transistor and PNP transistor, and rapid discharge of the read **bit line** is possible because of the high gain of this combination of components
DETAILED DESCRIPTION - A gain cell for a DRAM comprises; (a) MOSFET write transistor with its gate connected to be driven by a write **word line**, its drain connected to a storage node having a storage capacitor associated with it, and its source connected to a write **bit line**. (b) MOSFET read transistor with its gate connected to the storage node and its source connected to a read **word line**. (c) Bipolar transistor with its base connected to the drain of the read transistor and its emitter connected to a read **bit line**.
USE - DRAM fabrication.
ADVANTAGE - The DRAM has improved access and cycle time, the gain cells can operate for linger without a refresh operation and can read data in a non-destructive manner and require smaller storage capacitance. The DRAMs are larger and can be made cheaper.
DESCRIPTION OF DRAWING(S) - The drawings show a DRAM including;
storage capacitor Cs
storage node Vs
read **bit line** BLr
write **bit line** BLw
read **word line** WLAr
write **word line** WLAw
read **word line** WLBr
write **word line** WLBw
node X
gain cell 10
write device 12
bipolar PNP device 14
read device 16
P+ junction 30
N- well 32
polysilicon stud contact 35
N+ source diffusion area 36
gate 38.
Dwg.1,3/13

L31 ANSWER 3 OF 8 WPIX (C) 2002 THOMSON DERWENT
AN 1995-219028 [29] WPIX
DNN N1995-171799
TI Structure of semiconductor **DRAM** memory - has vertical **metal oxide semiconductor** transistor by setting up source and drain domain on either sides of channel, and trench capacitor.
DC U13 U14
IN OZAKI, T
PA (TOKE) TOSHIBA KK
CYC 2
PI JP 07130871 A 19950519 (199529)* 8p
US 5519236 A 19960521 (199626) 20p
ADT JP 07130871 A JP 1993-156453 19930628; US 5519236 A US 1994-266389 19940627

PRAI JP 1993-156453 19930628
AB JP 07130871 A UPAB: 19950727
The structure has a trench (12) formed by the regular arrangement of the DRAM cells on a **silicon** substrate (10). A capacitor is formed by laying an electrode (14) in the trench. A pillar (20) made up of **silicon** which adjoins the trench perpendicularly acts as the channel. A source domain (18) and a drain domain (24) set up on either sides of the channel constitute the vertical metal oxide semiconductor transistor of the semiconductor memory unit.
ADVANTAGE - Improves reliability of semiconductor memory. Does not require alignment substrate for manufacturing process. Reduces aspect ratio of pillar without reducing capacitance.
Dwg.9/13

L31 ANSWER 4 OF 8 WPIX (C) 2002 THOMSON DERWENT
AN 1992-375845 [46] WPIX
DNN N1994-072671
TI DRAM device with capacitor between vertically aligned FETs - stores two bit information in two access transistors one above having thin film transistor structure with capacitor sandwiched between transistors..
DC U13 U14
IN YANAGI, M
PA (SHAF) SHARP KK
CYC 2
PI JP 04274359 A 19920930 (199246)* 6p
US 5299155 A 19940329 (199412)B 11p
ADT JP 04274359 A JP 1991-34870 19910301; US 5299155 A Cont of US 1992-841522 19920226, US 1993-84442 19930701
PRAI JP 1991-34870 19910301
AB US 5299155 A UPAB: 19940510 ABEQ treated as Basic
The dynamic random access memory device is formed on a **silicon** substrate and comprises a first access transistor comprised of a first **word line** formed on the **silicon** substrate. A first **bit line** makes electrical contact with the first access transistor at a first contact region. A capacitor comprises a capacitor first electrode above the first access transistor. A dielectric film covers the first capacitor electrode and a capacitor second electrode covers the dielectric film.
A second access transistor includes a second **word line**. A second **bit line** makes electrical contact with the second access transistor at a second contact region.
USE/ADVANTAGE - **MOS Dram** devices. Memory cell area occupying substrate is greatly reduced without reducing capacitor electrode area.
Dwg.6/10
AB JP 04274359 A UPAB: 19981217
Dwg.2/9

L31 ANSWER 5 OF 8 WPIX (C) 2002 THOMSON DERWENT
AN 1984-198402 [32] WPIX
TI **MOS dynamic memory** - has **bit line** using multi-crystal **silicon** or metal, and gate electrode serving as **word line** NoAbstract Dwg 1a-d/2.
DC U13 U14
PA (TOKE) TOKYO SHIBAURA DENKI KK
CYC 1
PI JP 59113659 A 19840630 (198432)*
ADT JP 59113659 A JP 1982-223446 19821220
PRAI JP 1982-223446 19821220

L31 ANSWER 6 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1992-212450 JAPIO
TI SEMICONDUCTOR STORAGE DEVICE AND ITS MANUFACTURE
IN OZAKI KOJI
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 04212450 A 19920804 Heisei
AI JP1991-46782 (JP03046782 Heisei) 19910312
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1294, Vol. 16, No. 558, P. 2 (19921127)
AB PURPOSE: To realize the structure of a semiconductor storage device which does not constitute a parasitic MOS transistor as the result of microminiaturization of a memory cell, in a semiconductor storage device of high integration level and high density.
CONSTITUTION: A **DRAM** has an **MOS** transistor and a capacitor which are formed in a trench 3. The trench 3 is formed in an insulating film 2. The MOS transistor has a gate electrode (**word line**) 11 and n+ impurity regions 9, 14. The capacitor is provided with a cell blade composed of a p+ **silicon** substrate 1, a nitride film 4, and a storage node compose of an n+ poly **silicon** layer 5. All of the constituent elements of a memory cell are formed in the trench 3. The **word line** 11 and a **bit line** 17 are also formed in the trench 3.

L31 ANSWER 7 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1981-067960 JAPIO
TI **MOS DYNAMIC RANDOM** ACCESS **MEMORY**
IN FUJISHIMA KAZUYASU
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 56067960 A 19810608 Showa
AI JP1979-143478 (JP54143478 Showa) 19791105
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 70, Vol. 5, No. 1291, P. 164 (19810819)
AB PURPOSE: To prevent a noise during selecting a **word line** by a method wherein a transfer transistor in capacity coupling with a gate composing a capacitor of an **MOS dynamic RAM** and earthed to the ground through a resistor is installed.
CONSTITUTION: A memory cell is earthed to the ground through a resistor 10 or a transistor and is composed of an N+ diffusion layer 1 constituting a **bit line**, the 1st layer **polysilicon** gate 9 connected to a word storage line, a resistor 10 or a transistor, a grounded **word line** 8 of the 2nd layer **polysilicon** gate constituting a transfer transistor, a gate oxide film 4 and a field oxide film 5. The word storage line and the grounded **word line** are in a capacity coupling. And during selection of a word storage line, the grounded line deflects to a negative side owing to its capacity coupling, however, a noise is not induced at a **bit line**, thus, enabling a preparation of a large capacity memory.

L31 ANSWER 8 OF 8 JAPIO COPYRIGHT 2002 JPO
AN 1981-067959 JAPIO
TI **MOS DYNAMIC RANDOM** ACCESS **MEMORY**
IN FUJISHIMA KAZUYASU
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 56067959 A 19810608 Showa
AI JP1979-143476 (JP54143476 Showa) 19791105
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 70, Vol. 5, No. 1291, P. 164 (19810819)

AB PURPOSE: To prevent unequality of a cell capacitance by a method wherein a separating gate is used to separate a **word line** of an **MOS dynamic RAM** from a memory cell and an MOS capacitance is constituted with the 2nd layer **polysilicon** gate.
CONSTITUTION: An 1-transistor 1-capacitor type memory cell consists of an N+ diffusion area 11 constituting a **bit line**, the 1st layer **polysilicon** gate 12 constituting a **word line**, a separating gate 16 wherein a VSS voltage is applied to separate each memory cell one another, the 2nd layer **polysilicon** gate 13 constituting an MOS capacitor and a gate oxide film 14. And during the 1st layer **polysilicon** gate being formed, each of the gate are of a transfer transistor, the area of an MOS capacitor and the area of an N+ diffusion layer is decided and they are equal without depending upon an error of a mask matching, thus, resulting in each equal cell capacitance and each equal **bit line** capacitance.

L44 ANSWER 1 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2002-237009 [29] WPIX
DNN N2002-182317 DNC C2002-071681
TI Semiconductor substrate for dynamic random access memory, has buried oxide region formed at predetermined depth with respect to upper surface of substrate to form **silicon** layer of specific thickness.
DC L03 U11 U13
IN DAVARI, B; SADANA, D K; SHAHIDI, G G; TIWARI, S
PA (IBMC) INT BUSINESS MACHINES CORP
CYC 2
PI US 6333532 B1 20011225 (200229)* 18p
KR 2001029900 A 20010416 (200229)
ADT US 6333532 B1 US 1999-356295 19990716; KR 2001029900 A KR 2000-38803 20000707
PRAI US 1999-356295 19990716
AB US 6333532 B UPAB: 20020508
NOVELTY - A **silicon**-on-insulator (SOI) region (18) adjacent to semiconductor region, has a buried oxide region (17) which is parallel to the surface of the substrate (12). The buried oxide region is formed at a predetermined depth with respect to the upper surface of the substrate so as to form a **silicon** layer of specific thickness.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for a structure for forming electrical devices.

USE - For fabrication of complementary **metal oxide semiconductor** (CMOS) circuits, **dynamic** Random Access **memories** (**DRAMs**) etc.

ADVANTAGE - Since a **silicon** layer of specific thickness is formed, the crystalline dislocation and defects can be prevented from propagating into the substrate.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of the semiconductor structure.
Substrate 12
Buried oxide region 17
SOI region 18
Dwg.8/14

L44 ANSWER 2 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2002-143433 [19] WPIX
DNC C2002-044598
TI Titanium manufacture for aircraft, involves heat processing mixture of sponge titanium powder and titanium oxide powder, sintering such that circumference of sponge is sintered, melting and adjusting oxygen content.
DC M25 M26
PA (TOXI) TOHO TITANIUM CO LTD
CYC 1
PI JP 2001279345 A 20011010 (200219)* 8p
ADT JP 2001279345 A JP 2000-93558 20000330
PRAI JP 2000-93558 20000330
AB JP2001279345 A UPAB: 20020321
NOVELTY - The sponge titanium (Ti) powder of mean particle diameter 1-50 mm and titanium oxide (TiO_2) powder are mixed and heat processed at 600-1100 deg. C under reduced pressure in a heating container (1). The heated mixture is sintered such that only circumference of Ti sponge is sintered and the sintered sponge and TiO_2 powder are electron beam melted to manufacture titanium whose oxygen content is adjusted.

USE - For manufacture of titanium used as material of aircraft, target for sputterings, and barrier material, and in semiconductor industry for semiconductor element such as very large scale integration

(VLSI), for e.g. 16-64 M bit **dynamic** random access
memory (**DRAM**) and **silicon metal**
oxide semiconductor (MOS) memory.
ADVANTAGE - The oxygen content in titanium is adjusted desirably and stably, and impurities such as chlorine and magnesium in sponge titanium powder are separated efficiently. Dispersion of titanium oxide at the time of melting is prevented. Thereby, titanium with minimum impurity content, high stability and quality is manufactured simply and rapidly.
DESCRIPTION OF DRAWING(S) - The figure shows block diagram of heating container and cooling condensing plant. (Drawing includes non-English language text).
Heating container 1
Dwg.1/3

L44 ANSWER 3 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2002-065554 [09] WPIX
DNN N2002-048691 DNC C2002-019342
TI Contact vias and copper interconnect fabrication method for integrated circuits, involves depositing low dielectric material over **polysilicon** materials, planarizing excess materials and removing **polysilicon** lines and islands.
DC L03 U11
IN TAI, S; TU, A; YEU, T
PA (TASE-N) TAIWAN SEMICONDUCTOR MFG CO
CYC 1
PI US 6309957 B1 20011030 (200209)* 10p
ADT US 6309957 B1 US 2000-541489 20000403
PRAI US 2000-541489 20000403
AB US 6309957 B UPAB: 20020208
NOVELTY - The excess sacrificial **polysilicon** islands and low dielectric material sequentially deposited over wiring (16) and insulating layer (14) are planarized. Excess **polysilicon** lines and low dielectric layer sequentially formed over the **polysilicon** islands and low dielectric material are planarized. Trench interconnects (62) and contact through openings (60) are formed by removing lines and islands.
USE - The method is used for fabricating copper interconnects and contact vias in semiconductor integrated circuit devices e.g. metal oxide semiconductor field effect transistor (MOSFET), complementary **metal oxide semiconductor** (CMOS) and **dynamic** random access **memory** (**DRAM**) devices.
ADVANTAGE - The process of **polysilicon** etching, plasma ashing of patterning photoresist and post cleaning ensures high quality control over the fabrication of copper interconnects and contacts.
DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of semiconductor integrated circuit.
Insulating layer 14
Wiring 16
Openings 60
Trench interconnects 62
Dwg.1F/2

L44 ANSWER 4 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2001-579848 [65] WPIX
CR 2001-334607 [29]
DNN N2001-431660 DNC C2001-172041
TI Manufacture of integrated circuit, e.g. dynamic random access memory, involves forming layer of undoped semiconductive material with elevated source/drain material for transistor gate line.

DC L03 U11
IN AHMAD, A; JONES, L
PA (AHMA-I) AHMAD A; (JONE-I) JONES L
CYC 1
PI US 2001009791 A1 20010726 (200165)* 19p
ADT US 2001009791 A1 Cont of US 1998-203541 19981201, US 2001-771449 20010126
FDT US 2001009791 A1 Cont of US 6211026
PRAI US 1998-203541 19981201; US 2001-771449 20010126
AB US2001009791 A UPAB: 20011108
NOVELTY - An integrated circuit is made by forming a transistor gate line on a substrate (32). A layer of undoped semiconductive material (54) is formed laterally proximate the gate line (36, 38) and joins with semiconductive material of the substrate. It comprises elevated source/drain material. Conductivity-modifying impurity is provided into the elevated source/drain material.

USE - For making integrated circuit, e.g. **dynamic** random access **memory** (**DRAM**), complementary **metal oxide semiconductor** (CMOS), or metal oxide semiconductor field effect transistors (MOSFETs).

ADVANTAGE - The invention improves CMOS formation techniques which use plugs or elevated source/drain regions over the p+/n+ active areas followed by a salicide process for sheet resistance reductions which improves robustness in the finished device. It does not require a self-aligned contact etch to form DRAM cell capacitors. It can also achieve n-channel and p-channel devices with elevated source/drain regions for better short channel characteristics without the use of additional masking steps.

DESCRIPTION OF DRAWING(S) - The figure is a view of the semiconductor wafer fragment.
Substrate 32
Gate lines 36, 38
Insulating cap 44
Undoped semiconductive material 54
Patterned masking layer 58
Elevated source/drain regions 60, 62, 64
Dwg.5/19

L44 ANSWER 5 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2001-450377 [48] WPIX
CR 1999-120591 [10]
DNN N2001-333336 DNC C2001-135974
TI Production of enhanced purity, high-density, fine microstructure sputtering targets useful in semiconductor memory devices, involves utilizing the combination of reactive sintering and vacuum hot pressing.
DC L03 U11
IN KELLER, J A; MORALES, D L; SHAH, R P
PA (HONE) HONEYWELL INT INC
CYC 1
PI US 6258719 B1 20010710 (200148)* 11p
ADT US 6258719 B1 US 1998-108610 19980701
PRAI US 1998-108610 19980701
AB US 6258719 B UPAB: 20020725
NOVELTY - A sputtering target is produced by utilizing a combination of reactive sintering and vacuum hot pressing of aluminum or **silicon** powders.

DETAILED DESCRIPTION - Production of sputtering targets comprises in situ reactive sintering and hot pressing metal and aluminum powders. The metal powders can be titanium, iron, cobalt, nickel, or tantalum. The reactive sintering is performed by subjecting the powders at 500-1000 psi

for 60-240 minutes. The hot pressing is performed by subjecting the powders at 1000-6000 psi while heating the powders at 600-1500 deg. C.

USE - For producing sputtering targets, e.g., aluminide or silicide targets, useful in complementary **metal oxide semiconductor** (CMOS) **dynamic** random access **memory (DRAM)** devices.

ADVANTAGE - The invention is a one-step process for producing stoichiometric and non-stoichiometric, enhanced purity, high density, and fine microstructure sputtering targets.

Dwg.0/4

L44 ANSWER 6 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2001-158577 [16] WPIX
CR 1997-011225 [01]; 1997-434418 [40]; 1998-017586 [02]; 1998-285712 [25]; 1998-387045 [33]; 2000-349402 [29]; 2000-464329 [39]; 2002-225628 [75]
DNN N2001-115519
TI **Silicon** integrated circuit formation for dynamic random access memory and complementary metal oxide **silicon** circuits includes filling trench with dielectric material so that side walls are coated with dielectric material.
DC U11 U13 U14
IN RHODES, H E
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6177333 B1 20010123 (200116)* 12p
ADT US 6177333 B1 US 1999-231176 19990114
PRAI US 1999-231176 19990114
AB US 6177333 B UPAB: 20020502

NOVELTY - The integrated circuit fabrication includes forming an isolation trench (22) in the semiconductor substrate and partially filling the trench with dielectric material. The sidewalls (28) are coated with dielectric material. Ions are implanted into the substrate in regions directly below the isolation trench after partially filling the trench with the dielectric material (24).

DETAILED DESCRIPTION - The dielectric (24) along the sidewall of the trench can serve as a mask (30) so that all the ions implanted below the isolation trenches are displaced from the active regions. partially filling the trench includes forming a layer of **silicon** dioxide and the deposition of this material is by chemical vapor deposition. The implant depth is 20-80% of the depth of the trench.

USE - For use in memory devices, imaging devices, logic and semiconductor devices in **silicon** integrated circuits. These include **dynamic** random access **memory (DRAM)**, complementary **metal oxide semiconductor** (CMOS) imagers and charge coupled devices (CCD).

ADVANTAGE - The trench isolation technique can be used to fabricate a variety of integrated circuits which can include devices that exhibit reduced current leakage and/or reduced optical cross talk.

The dielectric along the sidewalls of the trench can serve as a mask so that all the ions implanted below the isolation trenches are displaced from the active region. The remainder of the trench can be filled with same or another dielectric material. The techniques can be used to provide isolation for an active region on any semiconductor device.

DESCRIPTION OF DRAWING(S) - The drawing shows a cross sectional view of an partially filled isolation trench which includes a layer of **silicon** dioxide.

Trenches 22

Dielectric material 24

Active ion regions 26

Trench walls 28
Photo resist mask 30
Dwg.4/10

L44 ANSWER 7 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2001-074664 [09] WPIX
DNN N2001-056830
TI Semiconductor device manufacturing method involves forming upper electrode on two capacitive insulating films which are sequentially on lower electrode connected to diffusion area of substrate.
DC U11 U13 U14
PA (NIDE) NEC CORP
CYC 1
PI JP 2000294752 A 20001020 (200109)* 15p
ADT JP 2000294752 A JP 1999-115538 19990422
PRAI JP 1999-26140 19990203
AB JP2000294752 A UPAB: 20010213
NOVELTY - Two capacitive insulating films (9,10) are formed sequentially on a lower electrode (8) which is connected to N-type diffusion area (5) on a P-type **silicon** substrate (1). The substrate with the electrode and film is heat treated in oxidizing atmosphere. An upper electrode (12) of capacitor is then formed on the films.
DETAILED DESCRIPTION - The lower and upper electrodes with the insulating films in between constitute a capacitor. The electrodes are made of are titanium nitride. The capacitive insulating films are tantalum oxide films.
USE - For manufacture of semiconductor devices such as static random access **memory**, **dynamic random** access **memory**, **metal oxide semiconductor** transistor.
ADVANTAGE - Prevents oxygen from reacting with the lower electrode and so oxidation of lower electrode is suppressed.
DESCRIPTION OF DRAWING(S) - The figure explains the manufacture of the semiconductor device.
P-type semiconductor substrate 1
N-type diffusion area 5
Lower electrode 8
Capacitive insulating films 9,10
Upper electrode 12
Dwg.2/20

L44 ANSWER 8 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2000-678771 [66] WPIX
CR 2001-089862 [63]; 2001-513048 [44]
DNN N2000-502442 DNC C2000-206369
TI Method and apparatus for dry etching where effective pumping speed of vacuum chamber is defined by specified parameters.
DC L03 U11
IN KUMIHASHI, T; TACHI, S; TSUJIMOTO, K
PA (HITA) HITACHI LTD
CYC 1
PI US 6136721 A 20001024 (200066)* 26p
ADT US 6136721 A CIP of US 1992-859336 19920327, Div ex US 1993-34126 19930318, CIP of US 1994-176461 19940103, Div ex US 1994-301388 19940907, Div ex US 1995-570689 19951211, Div ex US 1997-861600 19970522, Cont of US 1998-63406 19980421, US 2000-480477 20000111
FDT US 6136721 A CIP of US 5242539, Div ex US 5318667, CIP of US 5354418, Div ex US 5474650, Div ex US 5650038, Div ex US 5795832, Cont of US 6008133
PRAI JP 1992-68098 19920326; JP 1991-71464 19910404; JP 1992-3675

19920113; JP 1992-61736 19920319
AB US 6136721 A UPAB: 20020508
NOVELTY - Method and apparatus for dry etching semiconductor which changes one or both of effective pumping speed of vacuum chamber or gas flow rate, so as to alter the processing of an etching pattern side wall of a sample between first and second conditions.
DETAILED DESCRIPTION - The first and second conditions comprise the presence or absence of a deposit film, or the presence, absence or shape of a taper angle. the chamber is exhausted by using at least one pump where effective exhaust speed is 1/S = 1/ nSi + 1/C, where:
(1) S is the effective exhaust speed
(2) Si is an exhaust speed of one pump
(3) n is the number of pumps;
(4) C is the exhaust conductance of the chamber.
The effective exhaust speed of the chamber is not less than 600 liters/second. The gas pressure is not more than 25mTorr. The etching gas is chlorine or bromine. The semiconductor body comprises **silicon** , aluminium, tungsten, tungsten-silicide, copper, gallium-arsenide, **silicon** nitride, and titanium nitride.
USE - High anisotropic patterning dry etching process for production of **dynamic** random access **memory** (**DRAM**) or **MOS** transistor.
ADVANTAGE - Prevents over-etching during patterning and damaging components.
Dwg.0/15

L44 ANSWER 9 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2000-580984 [55] WPIX
DNN N2000-430069 DNC C2000-173090
TI Semiconductor device e.g., dynamic random access memory includes a baffler film formed under a high density plasma chemical vapor deposited **silicon** oxide layer.
DC L03 U11
IN CHAN, C; CHENG, L; MOGHADAM, F; MOGHADAM, F K
PA (MATE-N) APPLIED MATERIALS INC; (CHAN-I) CHAN C; (CHEN-I) CHENG L; (MOGH-I) MOGHADAM F K
CYC 28
PI EP 1039524 A2 20000927 (200055)* EN 8p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI
JP 2000307004 A 20001102 (200061) 19p
KR 2000076611 A 20001226 (200134)
US 2002000664 A1 20020103 (200207)
ADT EP 1039524 A2 EP 2000-300919 20000207; JP 2000307004 A JP 2000-29604 20000207; KR 2000076611 A KR 2000-5616 20000207; US 2002000664 A1 US 1999-245438 19990205
PRAI US 1999-245438 19990205
AB EP 1039524 A UPAB: 20001102
NOVELTY - The performance of a **silicon** oxide film deposited by high density plasma chemical vapor deposition is enhanced by providing a baffler film under the **silicon** oxide layer. The baffler film comprises a **silicon** nitride film deposited on a first dielectric film.
DETAILED DESCRIPTION - INDEPENDENT CLAIMS are also included for the following:
(a) a semiconductor device comprising:
(i) a **polysilicon** substrate (12);
(ii) a dielectric film (46) deposited on the **polysilicon** substrate;

(iii) a **silicon** nitride film (44) deposited on the dielectric film;
(iv) a silicate glass film deposited on the **silicon** nitride film; and
(v) a metal film deposited selectively over the silicate glass film; and
(b) a method of forming a semiconductor device on a substrate comprising:
(i) depositing a first dielectric film (46) over the substrate (12);
(ii) depositing a **silicon** nitride film (44) over the dielectric film;
(iii) depositing a silicate glass film over the **silicon** nitride film;
(iv) etching a via through the silicate glass, the **silicon** nitride and the dielectric films;
(v) depositing a metal interconnect (24) in the via;
(vi) depositing a metal film over the silicate glass film;
(vii) etching a section of the metal film to expose a section of the silicate glass film; and
(viii) depositing a **silicon** oxide film (26) over the silicate glass and metal films using high density plasma chemical vapor deposition (HDP-CVD) techniques.
USE - Semiconductor devices e.g., static random access memory (SRAM), complementary **metal oxide semiconductor** (CMOS) and **dynamic** random access **memory** (**DRAM**) devices.
ADVANTAGE - The performance of the **silicon** oxide films deposited by HDP-CVD is improved by providing a baffler layer under the **silicon** oxide layer to prevent diffusion into underlying structures, such as gates, and to minimize plasma induced damage.
DESCRIPTION OF DRAWING(S) - The diagram shows a cross sectional view of an advanced multilevel logic device.
Polysilicon substrate layer 12
Poly-metal dielectric layer 18
Boron and phosphorus doped silica glass 22
Metal interconnects 24
Silicon oxide layer 26
Baffler layer 42
Silicon nitride film 44
Tetra-ethyl-ortho-silicate film 46
Dwg.2/4

L44 ANSWER 10 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 2000-306690 [27] WPIX
DNN N2000-229333 DNC C2000-093408
TI Stopper film formation method for manufacture of DRAM, C-MOS device, involves using halogen compound of **silicon** and hydrogen gas of predefined density, to form **silicon** nitride film on polycrystalline **silicon** film.
DC L03 U11
PA (HITA) HITACHI LTD
CYC 1
PI JP 2000058483 A 20000225 (200027)* 7p
ADT JP 2000058483 A JP 1998-221323 19980805
PRAI JP 1998-221323 19980805
AB JP2000058483 A UPAB: 20000606
NOVELTY - A **silicon** oxide film (102) is formed on a single crystal **silicon** substrate (101). A boron doped polycrystalline **silicon** film (104) is formed on the **silicon** oxide film.

A **silicon** nitride film (105), which acts as a stopper film is formed on the **silicon** film (104), using nitrogen gas of predefined density, and a halogen compound of **silicon**.

USE - For **dynamic** random access **memory** (**DRAM**), complicated-**metal oxide semiconductor** (C-MOS) device.

ADVANTAGE - Reduces quantity of boron leaked from boron doped polycrystalline **silicon** film, by forming stopper layer.

DESCRIPTION OF DRAWING(S) - The figure shows the sectional view of semiconductor device.

Single crystal **silicon** film 101
Silicon oxide film 102
Silicon film 104
Silicon nitride film 105
Dwg.1/4

L44 ANSWER 11 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 1999-590619 [50] WPIX
CR 1997-258225 [23]
DNN N1999-435608 DNC C1999-172393
TI Semiconductor processing for forming complementary **metal oxide semiconductor** (CMOS) **dynamic** random access **memory** (**DRAM**).
DC L03 U13 U14
IN DENNISON, C; HELM, M
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 5970335 A 19991019 (199950)* 13p
ADT US 5970335 A Cont of US 1995-503199 19950717, US 1997-797547 19970207
FDT US 5970335 A Cont of US 5624863
PRAI US 1995-503199 19950717; US 1997-797547 19970207
AB US 5970335 A UPAB: 19991201

NOVELTY - The process involves forming complementary n-type doped and p-type doped active regions within a semiconductor substrate.

DETAILED DESCRIPTION - The method comprises

(i) defining a memory array area and a peripheral area of a semiconductor substrate,

(ii) forming first and second transistor gates over the peripheral area, the first gate to be utilized for the formation of an n-type field effect transistor (FET), the second gate to be utilized for the formation of a p-type FET,

(iii) defining first active regions adjacent the first gate and defining second active regions adjacent the second gate,

(iv) masking the first active regions while conducting p-type conductivity doping into the second active region,

(v) forming an insulating layer over the active regions,

(vi) forming voids through the insulating layer to the first active region,

(vii) filling the voids with n-type conductively doped **polysilicon** plugs having an n-type dopant impurity concentration of at least 1x1020 ions/cm3, the first active region having an n-type dopant concentration prior to the filling step of 0 - 1x1019 ions/cm3,

(viii) out-diffusing n-type dopant impurity from the n-type conductively doped **polysilicon** plugs into the substrate to increase the n-type dopant impurity concentration within the first active regions to at least 1x1020 ions/cm3, and

(ix) forming a series of DRAM cells within the array, the cells comprising a series of n-type FETs and associated capacitors.

USE - For the manufacture of semiconductor memory cells.

ADVANTAGE - The method facilitates the formation of complementary source and drain regions within a semiconductor substrate and minimizes the number of masking steps.

DESCRIPTION OF DRAWING(S) - The drawing shows the wafer during processing.

Implant regions 40
p-type implant regions 42
Photoresist 44
n-type implant regions 74
Dwg.10/11

L44 ANSWER 12 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 1996-418259 [42] WPIX
DNN N1996-352512
TI Semiconductor device for MOS dynamic RAM used in main memory of e.g. large computer - has **polysilicon** film and capacitor oxide film formed inside first conductive semiconductor substrate, and another **polysilicon** film formed inside capacitor oxide film.
DC U13 U14
PA (TOKE) TOSHIBA KK
CYC 1
PI JP 08204146 A 19960809 (199642)* 11p
ADT JP 08204146 A JP 1995-10026 19950125
PRAI JP 1995-10026 19950125
AB JP 08204146 A UPAB: 19961021
The device has a semiconductor substrate (21) with conductive quantity impurity density. A dielectric isolation substrate (26) is provided for a dynamic RAM. A dielectric film (22) is placed between the dielectric isolation substrate and another conductive semiconductor substrate (23). The DRAM has a selection transistor and a storage capacitor made of several arranged memory units.

The selection transistor is formed on the surface of the second semiconductor substrate. The storage capacitor is inserted to the dielectric film on the surface of the second semiconductor substrate. A **polysilicon** film (242) and a capacitor oxide film (243) are formed inside the first semiconductor substrate. Another **polysilicon** film (244) is formed inside the capacitor oxide film.

ADVANTAGE - Prevents ion implantation damage and generation of crystal defect since cell plate electrode of high concentration layer is not formed through ion implantation. Increases integration density of DRAM and prevents generation of trench defect thus improving productivity.
Dwg.1/15

L44 ANSWER 13 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 1994-361583 [45] WPIX
DNN N1994-283457 DNC C1994-164833
TI Semiconductor device mfr. - involving resin application on substrate according to pattern followed by angular ion implantation of boron impurity.
DC L03 U11 U13 U14
PA (SONY) SONY CORP
CYC 1
PI JP 06283675 A 19941007 (199445)* 5p
ADT JP 06283675 A JP 1993-65787 19930325
PRAI JP 1993-65787 19930325
AB JP 06283675 A UPAB: 19950102
The semiconductor device manufacturing method is applied to an n-type **silicon** substrate (1). The element separation insulation film (2) is formed on the surface of the substrate. Resin is then applied on the

substrate surface according to the pattern.
At this stage, the substrate is taken to a chamber suitable for ion implantation. The substrate is positioned in the stage and aligned. The ion implantation head is rotated so that the direction ion implantation makes a non zero angle with the vertical axis of the substrate. Ion implantation is executed using B+ ions.
USEDVANTAGE - For MOS integrated circuit production. Produces transistor with lower threshold voltage without increasing number production process steps. Provides wide application such as in CMOS analog switch, oscillator, DRAM amplifier, SRAM amplifier.
Dwg.2/12

L44 ANSWER 14 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 1994-231575 [28] WPIX
DNN N1994-183058 DNC C1994-105690
TI Solid state memory cells for dynamic random access memory - consists of combination of metal oxide semiconductor transistor and pipe-form node electrode.
DC L03 U11 U13 U14
PA (NIDE) NEC CORP
CYC 1
PI JP 06169068 A 19940614 (199428)* 6p
ADT JP 06169068 A JP 1992-319615 19921130
PRAI JP 1992-319615 19921130
AB JP 06169068 A UPAB: 19940831
The solid state memory cell has a P type **silicon** substrate (1). An element separation insulation film (2) separates the gates of a field effect transistor electrode (3) from the **silicon** substrate. N type node diffusion and bit diffusion layers (5, 6) are formed on the P substrate. Gates of a FET insulation film (4) separates the FET electrode from the diffusion and bit layers. A bit contact hole (7) is made to pass a bit ray (8). An insulation layer is formed (10) on the bit ray. Boron silicate glass film is formed (11) on the insulation layer. N type polycrystal **silicon** film is formed on the diffusion layer (5). Capacity insulation film (17) and cell plate electrode (18) are formed on it.
ADVANTAGE - No cracks since it does not use a **silicon** nitriding film. Hydrogenation processing for decreasing a boundary face level is performed fully.
Dwg.1/4

L44 ANSWER 15 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 1988-123274 [18] WPIX
TI MOS dynamic RAM to increase memory capacity - has **silicon** substrate with trench and has diffusion layer and cell plate NoAbstract Dwg 2,3/3.
DC U13 U14
PA (MITQ) MITSUBISHI DENKI KK
CYC 1
PI JP 63067768 A 19880326 (198818)* 8p
ADT JP 63067768 A JP 1986-213106 19860909
PRAI JP 1986-213106 19860909

L44 ANSWER 16 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 1984-209937 [34] WPIX
TI Double-layer poly **silicon** structure semiconductor memory element - is for MOS dynamic RAM cell, having high immunity to alpha rays and external noises NoAbstract Dwg 1/5.
DC U13 U14

PA (OKID) OKI ELECTRIC IND CO LTD
CYC 1
PI JP 59121866 A 19840714 (198434)* 6p
ADT JP 59121866 A JP 1982-227296 19821228
PRAI JP 1982-227296 19821228

L44 ANSWER 17 OF 17 WPIX (C) 2002 THOMSON DERWENT
AN 1981-75424D [41] WPIX
TI IC with MOSFET and capacitor - has one capacitor plate formed in substrate and other of poly **silicon** doped with MOS gate source and drain.
DC L03 U11 U12 U13 U14
IN BOETTCHER, C E; KLEIN, T; VARADI, G
PA (NASC) NAT SEMICONDUCTOR INC
CYC 1
PI US 4290186 A 19810922 (198141)* 10p
PRAI US 1977-788872 19770419; US 1979-59637 19790723; US 1981-280984 19810706
AB US 4290186 A UPAB: 19930915
The IC is made by (a) forming a first type region (18) in a first type substrate (10) of higher resistivity, (b) forming a shallow opposite type region (24) in the first region, as one capacitor plate, (c) forming an insulating layer (12) over substrate and regions, including portions serving as gate oxide and capacitor dielectric, (d) forming a polySi layer (26) on the insulator, having portions over the opposite type region, to be used as second capacitor plate, and over a substrate region spaced from it, to be used as self-aligned gate electrode, (e) forming openings in the insulator on opposite sides of the gate electrode and (f) doping source and drain regions (29,31) and simultaneously doping the gate electrode and second capacitor plate to render them conductive.

The structure is useful in single device **MOS memory** cell for **dynamic RAMs**. The capacitor can be formed in p-type substrates for fast devices and provides high capacitance/unit area, with the shallow junction minimising space requirements and the first type region preventing inversion layer formation.
3H,3I

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L49  ANSWER 1 OF 2  WPIX (C) 2002 THOMSON DERWENT
AN   1992-152727 [19]   WPIX
DNN  N1992-113941         DNC C1992-070614
TI   Stacked capacitor DRAM cell - has node electrode formed of
     alternate first and second conductor films with alternating indentations.
DC   L03 U11 U13 U14
IN   SAEKI, T; SATO, N
PA   (NIDE) NEC CORP; (NIDE) NEC KK
CYC  6
PI   EP 484088     A  19920506 (199219)* EN   23p
        R: DE FR GB
     JP 04278578   A  19921005 (199246)        5p
     JP 05006976   A  19930114 (199307)       12p
     US 5416037    A  19950516 (199525)       21p
     US 5504704    A  19960402 (199619)       20p
     EP 484088     B1 19960508 (199623)  EN   15p
        R: DE FR GB
     DE 69119354   E  19960613 (199629)
     KR 9616837    B1 19961221 (199931)
ADT  EP 484088 A EP 1991-309956 19911029; JP 04278578 A JP 1991-41474 19910307;
     JP 05006976 A JP 1991-277833 19911024; US 5416037 A Div ex US 1991-784269
     19911029, Cont of US 1993-145508 19931104, US 1994-299885 19940901; US
     5504704 A US 1991-784269 19911029; EP 484088 B1 EP 1991-309956 19911029;
     DE 69119354 E DE 1991-619354 19911029, EP 1991-309956 19911029; KR 9616837
     B1 KR 1991-19264 19911029
FDT  DE 69119354 E Based on EP 484088
PRAI JP 1990-291538    19901029; JP 1991-41474     19910307
AB   EP    484088 A UPAB: 19931006
       DRAM device includes a node electrode connected to a node
     diffusion layer in a semiconductor substrate and or stacked dielectric
     film, the electrode consisting of alternate stacked first and second
     conductor films, the ends of the first films being more indented than the
     ends of the second films.
          Pref. the first film is n-polySi and the second is O2-rich n-polySi
     or a refractory silicide.
          USE/ADVANTAGE - As the node electrode of a DRAM stacked
     capacitor. The indentations increase the surface area of the node
     electrode so that the capacitance of the capacitor is increased without
     any increase in device area occupied.  (2E/8)
     2E/8

L49  ANSWER 2 OF 2  JAPIO  COPYRIGHT 2002 JPO
AN   1983-063160    JAPIO
TI   MOS DYNAMIC MEMORY CELL
IN   KIMATA MASAAKI; SHIMOTORI KAZUHIRO; FUJISHIMA KAZUYASU
PA   MITSUBISHI ELECTRIC CORP, JP   (CO  000601)
PI   JP 58063160 A  19830414 Showa
AI   JP1981-161606 (JP56161606 Showa) 19811009
SO   PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No.
     185, Vol. 7, No. 1541, P. 73 (19830706)
AB   PURPOSE: To obtain an MOS dynamic memory
     capable of obtaining a large signal at a high speed by controlling a
     cell-plate voltage with a word line signal in a
     1-transistor MOS dynamic RAM.
     CONSTITUTION: A cell-plate electrode 8' is formed after a gate electrode 5
     during the manufacturing steps. After the electrode 5 is formed, an N type
     region 11 is formed with the electrode 5 as a mask. Accordingly, the
     region 11 is connected to a channel formed under the electrode 5.
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Accordingly, the region corresponding to the high density N type region in the conventional one can be eliminated. After an interlayer insulating film (normally **silicon** oxidized film) for insulating between the electrode 5 and the plate 8' after forming the N type region, the electrode 8' is formed. Since the high density N type region between the plate electrode and the transfer gate electrode can be eliminated, one side can be shortened by 2-5.theta.m as compared with the conventional memory cell, thereby enabling to perform high density.

L57 ANSWER 1 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2002-223831 [28] WPIX
DNN N2002-171300 DNC C2002-068333
TI Fabrication of self-aligned contact in an embedded dynamic random access memory involves forming a dielectric layer and contact holes in memory and logic regions of a substrate until source/drain regions are exposed.
DC L03 U11 U12 U13
IN CHEN, J; LIN, Y
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 6200848 B1 20010313 (200228)* 11p
ADT US 6200848 B1 US 1998-208612 19981208
PRAI US 1998-208612 19981208
AB US 6200848 B UPAB: 20020502

NOVELTY - **Metal oxide semiconductors** and source/drain regions are formed in memory and logic regions of a substrate. Dielectric layer and contact holes are formed in memory and logic regions until source/drain regions are exposed. Silicide layers are formed over contact holes and an interlayer dielectric is formed. Conductive vias are formed in memory and logic regions, and self-aligned contact is formed.

DETAILED DESCRIPTION - Fabricating a self-aligned contact, where a substrate (500) having a memory region (504) and a logic region (506) is provided, and **metal oxide semiconductors** (**MOS**) are respectively formed in the memory region (504) and in the logic region (506), comprises:

(a) forming as defined dielectric layer on the substrate (500);

(b) forming a first contact hole (522a) in the dielectric layer in the memory region, and simultaneously forming a second contact hole (522b) in the logic region until the substrate (500) is exposed;

(c) forming a first silicide layer (524a) over the first contact hole (522a) and a second silicide layer (524b) over the second contact hole (522b), respectively, to couple electrically the first and second silicide layers (524a, 524b) to the substrate (500), where portions of the first and second silicide layers (524a, 524b) extend to the surface of the dielectric layer neighboring the first and second contact holes;

(d) forming a defined interlayer dielectric (526) over the substrate (500);

(e) forming a first via in the logic region (506) to expose the first silicide layer (524a) and a second via in the memory region (504) until the second silicide layer (524b) is exposed; and

(f) forming a first metal (preferably tungsten) plug in the first via and a second metal plug in the second via, respectively, to couple the first and second silicide layers.

The first and second silicide layers (524a, 524b) can be titanium silicide or they can be cobalt silicide, and they are formed by a sputtering or chemical vapor deposition process.

USE - Dynamic random access memory manufacture.

ADVANTAGE - The invention overcomes the difficulties of forming and aligning a contact hole, because the thickness of dielectric layers in a memory region and in a logic region are very different.

DESCRIPTION OF DRAWING(S) - The drawing show a cross-sectional view of a self-aligned contact formed in an **embedded DRAM**, according to an embodiment of the invention.

Semiconductor substrate 500
Shallow trench isolation structure 502
Memory region 504

Logic region 506
    Gate structure 508
    Source/drain regions 510, 514
    Dual gate structure 512
Oxide layer 516
    Hard material layer 518
    Dielectric layer 520
    Contact holes 522a, 522b
    Patterned silicide layers 524a, 524b
    Interlayer dielectric layer 526
    Metal plugs 528a, 528b
Dwg.5D/5

L57 ANSWER 2 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2002-009161 [01] WPIX
DNN N2002-007604 DNC C2002-002142
TI **Embedded DRAM** self-aligned contact with borderless contact and method for making the same - comprises providing an **embedded DRAM** built on a substrate including a logic region and a memory region, etc..
DC L03 U11 U14
IN CHEN, D
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI TW 436986 A 20010528 (200201)*
ADT TW 436986 A TW 1999-109876 19990614
PRAI TW 1999-109876 19990614
AB TW 436986 A UPAB: 20020105
NOVELTY - A method for making a semiconductor device comprises providing an **embedded DRAM** built on a substrate including a logic region and a memory region, the logic region is formed with a **MOS** transistor and each of both sides of the logic region has a shallow trench isolation, the memory region is formed with a **MOS** transistor and each of both sides of the memory region has a shallow trench isolation (STI); forming a silicide barrier layer on the memory region to prevent the formation of a silicide on the substrate in the memory region; forming a silicide on the substrate of the logic region, and depositing a silicon nitride layer as an etching stop of a borderless contact; using a photoresist layer to remove the etching stop layer of the borderless contact in the memory region; forming a first inter-polysilicon dielectric layer (IPDI) on the upper layer of the substrate, and defining a pattern and etching out a self-aligned bit-line contact on the self-aligned silicized layer in the memory region; forming a second inter-polysilicon dielectric layer (IPD2) on the upper layer of the substrate, and defining a pattern and etching out a self-aligned node contact on the first IPDI in the memory region; forming an inter-dielectric material layer (ILD) on the upper layer of the substrate, and forming a third contact, a fourth contact and a fifth contact in the logic region; forming a borderless contact in the third contact and the fifth contact, and forming a metal layer (M1) on the top of the contact of the substrate.
Dwg.1/1

L57 ANSWER 3 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2001-217107 [22] WPIX
DNN N2001-154617
TI Manufacturing method for self-alignment contact (SAC) in **embedded DRAM**, defining both memory region and logic regions on the substrate.

DC U11 U13 U14
IN CHEN, S; LIN, Y
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI TW 396533 A 20000701 (200122)*
ADT TW 396533 A TW 1998-113405 19980814
PRAI TW 1998-113405 19980814
AB TW 396533 A UPAB: 20010421
NOVELTY - The method defines both memory region and logic regions on the substrate, where **MOS** structure and source/drain regions would be formed. Furthermore, dielectric film is defined on the substrate. A metal silicide is transformed into memory region and logic region respectively to release a contact opening with the exposed source/drain zones.
DETAILED DESCRIPTION - A metal silicide will cover the contact opening when the part of silicide extends to the dielectric surface. Later, a definite inner dielectric layer will be formed on the substrate, which is transformed into a dielectric opening on the memory region and logic region respectively. The metal layer is filled up to complete the SAC process.
Dwg.0/0

L57 ANSWER 4 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2001-008730 [02] WPIX
DNN N2001-006441
TI Voltage buffering arrangement in dynamic CMOS memory, i.**e**. **DRAM** - includes n-conductive tub structure supplied with higher voltage than p-conductive semiconductor area and p-conductive semiconductor substrate, whereby voltage to be buffered is applied at tub structure.
DC U13 U14 U21
IN SCHNEIDER, H; ZIBERT, M
PA (SIEI) INFINEON TECHNOLOGIES AG
CYC 1
PI DE 19946201 C1 20001214 (200102)* 4p
ADT DE 19946201 C1 DE 1999-19946201 19990927
PRAI DE 1999-19946201 19990927
AB DE 19946201 C UPAB: 20010110
The arrangement includes a p-conductive semiconductor substrate (7), an n-conductive tub structure (5, 6) provided in the semiconductor substrate, a p-conductive semiconductor area
(4) included by the tub structure, and an **NMOS** transistor
(1)
provided in the p-conductive semiconductor area. The n-conductive tub structure is supplied with a higher voltage than the p-conductive semiconductor area and the p-conductive semiconductor substrate.
The semiconductor substrate is put at a low supply voltage (VSS) and the tub structure at a high supply voltage, so that a voltage to be buffered is applied at the tub structure. The voltage to be buffered may be a negative word conductor blocking voltage or an amplified word conductor voltage.
ADVANTAGE - Provides adequate buffering capacity without additional space requirements.
Dwg.1/3

L57 ANSWER 5 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2000-450787 [39] WPIX
DNN N2000-335535
TI Test circuit of DRAM for computer system compares read data of memory with

expected data signal and latches error signal.
DC S01 U11 U13 U14 U21
IN MORGAN, D M; VO, H T
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6072737 A 20000606 (200039)* 19p
ADT US 6072737 A US 1998-130632 19980806
PRAI US 1998-130632 19980806
AB US 6072737 A UPAB: 20000818

NOVELTY - An external terminal receives test signal. Several comparison circuits (28) compare binary values of read data of memory (18) with expected data signal. A shift register circuit (38) latches the error signal output by comparator circuit and transfers it to data terminal (D2). A test control circuit (36) controls the operations of comparison circuit external terminal and shift register circuit.

DETAILED DESCRIPTION - If the compared signals of comparator have same binary values, an inactive error signal is output else an active error signal is output to shift register circuit. The test control circuit is coupled to external terminal, comparison circuit and shift register circuit. An INDEPENDENT CLAIM is also included for memory cells testing method.

USE - For testing **embedded DRAM** used in high resolution graphic system.

ADVANTAGE - Lower power consumption and electromagnetic radiation are attained. Noise and propagation delays are eliminated.

DESCRIPTION OF DRAWING(S) - The figure shows the functional block diagram of test system with **embedded DRAM**.

Memory 18
Comparison circuit 28
Test control circuit 36
Shift register circuit 38
Dwg.2/7

L57 ANSWER 6 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 2000-246117 [21] WPIX
DNN N2000-184064
TI Internal address and data path lines architecture used in memory cell array of **embedded DRAM**, has complementary pairs of digit and word lines formed in array region coupled to respective cells in associated column.
DC U13 U14
IN BUNKER, L; SHIRLEY, B
PA (MICR-N) MICRON TECHNOLOGY INC
CYC 1
PI US 6034900 A 20000307 (200021)* 15p
ADT US 6034900 A US 1998-146926 19980902
PRAI US 1998-146926 19980902
AB US 6034900 A UPAB: 20000502

NOVELTY - Several complementary pairs of digit lines and word lines (WL1-WLN) are formed in array region (206) and coupled to memory cells (208) in an associated column. Sense amplifiers (SA1-SAN) are formed in an amplifier region (218) of substrate adjacent to the array region and are coupled to respective pair of digit line, to which input-output lines (I/O1-I/OX) formed above array region are coupled.

DETAILED DESCRIPTION - At least one column select line (CSEL1,CSEL2) is formed above sense amplifier region, of which each line is coupled to a control input of the switches of respective amplifiers. Each switch includes **NMOS** transistors (220). The memory cell includes 512 I/O lines and two column select lines.

USE - For use in memory cell array of **embedded DRAM**
, SLDRAM used in computer systems.
ADVANTAGE - Provides high speed by using memory banks. Enables formation of wide data path without increasing the size of array or sense amplifier regions. The fabrication of **embedded DRAM** is possible due to advances in design and fabrication of ICs, resulting in significant reduction in size of transistors and other components.
DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of DRAM.
Array region 206
Memory cell 208
Amplifier region 218
NMOS transistor 220
Column select lines CSEL1,CSEL2
Input-output lines I/O1-I/OX
Sense amplifiers SA1-SAN
Word lines WL1-WLN
Dwg.2/6

L57 ANSWER 7 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 1999-633453 [54] WPIX
DNN N1999-467748
TI Low voltage generator for dynamic random access memory (DRAM) bit lines.
DC U13 U14
IN KALNITSKY, A; POPLEVINE, P
PA (SGSA) STMICROELECTRONICS INC
CYC 1
PI US 5982676 A 19991109 (199954)* 10p
ADT US 5982676 A US 1998-85559 19980526
PRAI US 1998-85559 19980526
AB US 5982676 A UPAB: 19991221
NOVELTY - The low voltage generator has a cascode circuit with a pair of series-connected **NMOS** transistors (16,18) and connected to a current generator (20). The output of the cascode circuit controls the potential of the bit lines of a memory array. A sense amplifier (3) with pass transistors (5) is interposed between the cascode circuit and the memory array.
USE - The low voltage generator is used for **embedded DRAM** array bit lines.
ADVANTAGE - Improves the performance of DRAM arrays by providing a controlled voltage to the bit lines and preventing unacceptable levels of charge leakage through the access transistors.
DESCRIPTION OF DRAWING(S) - The figure represents a schematic illustration of an **NMOS** cascode circuit employed to generate a controlled voltage on a bit line.
Sense amplifier 3
Pass transistors 5
NMOS transistors 16,18
Current generator 20
Dwg.1/5

L57 ANSWER 8 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 1999-470265 [40] WPIX
DNN N1999-351205 DNC C1999-138187
TI **Embedded DRAM** produced by simplified, reduced cost process.
DC L03 U11 U13 U14
IN HSIA, L; WU, H; HSIA, L C; WU, H J; SHIA, L
PA (UNIN-N) UNITED INTEGRATED CIRCUITS CORP; (LIAN-N) LIANLUI CLOSED CIRCUIT

CO LTD; (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 7
PI DE 19822797 A1 19990826 (199940)* 6p
FR 2775122 A1 19990820 (199940)
GB 2337160 A 19991110 (199949)#
JP 11261030 A 19990924 (199951) 7p
NL 1009204 C2 19991122 (200006)#
GB 2337160 B 20000329 (200019)#
US 6048762 A 20000411 (200025)
TW 444372 A 20010701 (200220)
DE 19822797 C2 20020411 (200223)
ADT DE 19822797 A1 DE 1998-19822797 19980520; FR 2775122 A1 FR 1998-6531 19980525; GB 2337160 A GB 1998-9771 19980507; JP 11261030 A JP 1998-144408 19980526; NL 1009204 C2 NL 1998-1009204 19980519; GB 2337160 B GB 1998-9771 19980507; US 6048762 A US 1998-55577 19980406; TW 444372 A TW 1998-102008 19980213; DE 19822797 C2 DE 1998-19822797 19980520
PRAI TW 1998-102008 19980213; GB 1998-9771 19980507; NL 1998-1009204 19980519
AB DE 19822797 A UPAB: 19991004

NOVELTY - An **embedded DRAM** is produced by a double damascening method, in which contact windows of different depth are formed in a single dielectric layer.

DETAILED DESCRIPTION - An **embedded DRAM** is produced by:

(a) preparing a substrate with a **MOS** element including a gate and a source/drain region and covered with a planarized dielectric layer;

(b) successively structuring the dielectric layer to form metal connection regions which expose the substrate, separate capacitor connection and bitline connection contact windows of the same depth and at the same plane for exposing the source/drain region and a logic circuit connection contact window of different depth for exposing the gate;

(c) successively forming a barrier layer and a second dielectric layer;

(d) structuring the second dielectric layer so that only the capacitor connection contact window and its associated metal connection region are covered;

(e) applying a metal layer; and

(f) planarizing the metal layer and the barrier layer using the first dielectric layer as etch-stop.

USE - For production of an **embedded DRAM**.

ADVANTAGE - The process employs a double damascening method, in which contact windows of different depth are formed in only one dielectric layer and in which the metal layer formed within the metal connection regions can be used as connections without further processing. Thus, the process is simplified and has reduced costs.

DESCRIPTION OF DRAWING(S) - The figure shows a cross-sectional view of an **embedded DRAM** at an intermediate stage of the production process.

substrate 10
gate 12
source/drain region 14
spacer layer 16
first dielectric layer 18
metal connection regions 20
capacitor connection contact window 22
bitline connection contact window 24
logic circuit connection contact window 26

Dwg.1D/1

L57 ANSWER 9 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 1999-394747 [33] WPIX
DNN N1999-295069 DNC C1999-115951
TI Manufacture of integrated circuit devices such as high speed processing circuits, embedded circuits e.g. **embedded DRAMs**, mixed mode circuits and other circuits incorporating FETs.
DC L03 U11 U13
IN SUN, S; TSAI, M
PA (UNMI-N) UNITED MICROELECTRONICS CORP
CYC 1
PI US 5920779 A 19990706 (199933)* 13p
ADT US 5920779 A Provisional US 1997-47252P 19970521, US 1997-903595 19970731
PRAI US 1997-47252P 19970521; US 1997-903595 19970731
AB US 5920779 A UPAB: 19990819

NOVELTY - Different thicknesses of gate oxide (46) are formed on a single chip.

DETAILED DESCRIPTION - Forming an IC device comprises:

(a) providing a semiconductor substrate (10) with first and second regions on which **MOS** devices are to be formed;

(b) masking the second region and providing a first concentration of a first dopant in the substrate at the surface of the first region without doping the second region;

(c) removing the mask over the second region;

(d) masking the first region and providing a second concentration of a second dopant in the substrate at the surface of the second region without doping the first region;

(e) oxidizing (46) the surface of the substrate to grow a first thickness of oxide on the first region of the substrate and growing a second, different thickness of oxide on the second region in a single oxidizing process; and

(f) forming **MOS** devices on the two regions.

USE - Manufacture of integrated circuit devices such as high speed processing circuits, embedded circuits e.g. **embedded DRAMs**, mixed mode circuits and other circuits incorporating FETs with different thicknesses of gate oxides on a single chip.

ADVANTAGE - The substrate is subjected to only one high temperature oxidation step therefore the process is simplified and shortened.

DESCRIPTION OF DRAWING(S) - The drawing shows a processing circuit with **embedded DRAM** incorporating different thicknesses of gate oxide.

Substrate 10
Gate oxide layer 46
Capacitor electrodes 102,104,108
Dwg.6c/6

L57 ANSWER 10 OF 12 WPIX (C) 2002 THOMSON DERWENT
AN 1998-387021 [33] WPIX
DNN N1998-301805 DNC C1998-116994
TI Embedded dynamic random access memory (DRAM) cells - fabricated using protection of metallic transistor contact plugs from the oxygen annealing of high dielectric constant dielectric capacitors.
DC L03 U11 U12 U13 U14
IN JIANG, B; JONES, R E; WHITE, B E; ZURCHER, P
PA (MOTI) MOTOROLA INC
CYC 2
PI US 5773314 A 19980630 (199833)* 11p
JP 10303398 A 19981113 (199905) 10p
ADT US 5773314 A US 1997-845457 19970425; JP 10303398 A JP 1998-125234

19980420
PRAI US 1997-845457 19970425
AB US 5773314 A UPAB: 19980819
A DRAM embedded structure with tungsten plugged **MOS** transistor devices is fabricated by; forming tungsten plugs (46) and bit line tungsten plugs (44) with a bottom capacitor electrode (48b) to protect the plug (46). Simultaneously an optionally removable barrier region (48a) is formed to protect the bit line plug (44). Capacitor dielectric (52) is deposited and oxygen annealed to form a ferroelectric capacitor material when the barrier (48a) and the lower electrode (48b) protect the tungsten plugs from oxidation. A top electrode layer (54,56) is then deposited, patterned , and etched when the barrier (48a) is removed. Interlayer dielectric (58) and contact plugs (60) are then formed to complete the structure. The barrier and bottom electrode (48a,b) are typically sputter deposited iridium which is etched using ion milling
USE - Fabrication of **embedded DRAMs**.
ADVANTAGE - Embedded ferroelectric DRAM capacitors which require an oxygen anneal can be achieved without oxidation of the tungsten metal plugs.
Dwg.7/8

L57 ANSWER 11 OF 12 JAPIO COPYRIGHT 2002 JPO
AN 1997-134598 JAPIO
TI SEMICONDUCTOR MEMORY DEVICE
IN WATANABE NAOYA; DOSAKA KATSUMI
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 09134598 A 19970520 Heisei
AI JP1995-290025 (JP07290025 Heisei) 19951108
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 97, No. 5
AB PURPOSE: TO BE SOLVED:To provide a DRAM (a general-purpose dynamic random-access memory) in which a control signal during the input/output of data can be output to the outside from an input/output terminal.
CONSTITUTION: **cache DRAM**, a DRAM 2 and an SRAM (a high-speed static random-access memory) 4 are integrated in one chip, and the respective memories are controlled by a control circuit 8 and a control circuit 6. In an ordinary operating mode, data from the memory (SRAM) 4 and the memory (DRAM) 2 are output to an output buffer 10 as they are. However, when a signal .vphi.tm at 'H' is input, a test mode is set, an output circuit 24 degenerates read-out data, and a control signal which controls a memory from which data is not read out is output, via the input/output buffer 10, to an input/output terminal 11 which becomes a surplus.

L57 ANSWER 12 OF 12 JAPIO COPYRIGHT 2002 JPO
AN 1995-169271 JAPIO
TI SEMICONDUCTOR STORAGE DEVICE, CLOCK-SYNCHRONOUS TYPE SEMICONDUCTOR DEVICE AND OUTPUT CIRCUIT
IN ABE HIDEAKI; OMOTO TOSHIYUKI; DOSAKA KATSUMI; KUMANOTANI MASAKI
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 07169271 A 19950704 Heisei
AI JP1993-310130 (JP05310130 Heisei) 19931210
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 95, No. 7
AB PURPOSE: To provide a **cache DRAM** provided with a command register capable of driving an output control signal at a high speed, storing the command data specifying many operation modes and internal conditions in a smaller occupation area and writing/reading from the outside.

CONSTITUTION: A control signal output circuit 50 is provided with a first output drive transistor PD conducting according to a drive signal .vphi.1 and discharging an output node 60 to a grounded potential level and a pull-up drive control circuit 72 generating a pull-up drive control signal becoming an activated state for a prescribed period when the first drive signal is inactivated. Further, the circuit 50 is provided with a pull-up drive circuit 74 becoming the activated state for the prescribed period according to the pull-up drive control signal and a second output transistor PU conducting in response to a drive signal .vphi.2 from the pull-up drive circuit 74 and driving the output node 60 to a power source potential level for the prescribed period. Then, even when the output node 60 is wired-OR-connected to a signal line, the circuit 50 is made the inactivated state at a high speed by the drive transistor PU at the time of inactivation.

L62 ANSWER 1 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2002-373587 [41] WPIX
DNN N2002-292006 DNC C2002-105793
TI Semiconductor memory device comprises a **metal oxide semiconductor** transistor having an electrically isolated floating bulk region.
DC L03 U13 U14
IN OHSAWA, T
PA (TOKE) TOSHIBA KK; (OHSA-I) OHSAWA T
CYC 27
PI EP 1180799 A2 20020220 (200241)* EN 93p
R: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI TR
US 2002051378 A1 20020502 (200241)
ADT EP 1180799 A2 EP 2001-119605 20010817; US 2002051378 A1 US 2001-917777 20010731
PRAI JP 2001-180633 20010614; JP 2000-247735 20000817; JP 2000-389106 20001221
AB EP 1180799 A UPAB: 20020701

NOVELTY - A memory cell (MC) comprises a **MOS** transistor that has a first data state in which majority carriers produced by impact ionization are injected and held in a floating bulk region (12) of the transistor, and a second threshold state in which the majority carriers in the bulk region are emitted by a forward bias at a p-n junction on the drain side as binary data.

DETAILED DESCRIPTION - The semiconductor memory device comprises at least one transistor that has a floating semiconductor layer (12) electrically isolated from other memory cells, a gate electrode (13) connected to a **word line** (WL), a drain diffusion region (14) connected to a **bit line** (BL), and a source diffusion region (15) connected to a fixed potential line (SL).

The semiconductor layer (12) is of a first conductivity type, and the drain and source diffusion regions are of a second conductivity type.

The transistor has a first data state having a first threshold voltage in which excessive majority are held in the semiconductor layer and a second data state having a second threshold voltage in which the excessive majority carriers in the semiconductor layer are emitted.

The first data state is one in which impact ionization is generated near a drain junction by operating the transistor and in which excessive majority carriers produced by the impact ionization are held in the semiconductor layer (12).

The second state is one in which a forward bias is applied between the semiconductor layer and the drain diffusion region to extract the excessive majority carriers from within the semiconductor layer (12) to the drain diffusion region.

The semiconductor layer (12) is preferably a p-type **silicon** layer formed on a **silicon** substrate (10) with an intermediate insulating film (11).

The transistor is preferably an N-channel **MOS** transistor.

INDEPENDENT CLAIMS are given for further semiconductor memory devices outlining further aspects of the invention, and methods for manufacture of the semiconductor device.

USE - **Dynamic** semiconductor **memory** (**DRAM**) device.

ADVANTAGE - The simple transistor structure used as a **memory** cell enables **dynamic** storage of binary data by a mall number of signal lines.

DESCRIPTION OF DRAWING(S) - The drawing shows a sectional view of the

structure of a **DRAM** memory cell according to a first embodiment
of the invention.
Silicon substrate 10
Insulating film 11
Semiconducting layer (Floating bulk region) 12
Gate electrode 13
Drain diffusion region 14
Source diffusion region 15
Gate oxide film 16
Bit line BL
Memory cell MC
Fixed potential source line SL
Word line WL
Dwg.1/71

L62 ANSWER 2 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 2000-095938 [08] WPIX
CR 1999-166666 [14]
DNN N2000-074025 DNC C2000-027887
TI Fabrication system for **dynamic random** access
memory (DRAM) cell.
DC L03 U13 U14
IN CHI, M
PA (VANG-N) VANGUARD INT SEMICONDUCTOR CORP
CYC 1
PI US 5998820 A 19991207 (200008)* 16p
ADT US 5998820 A Div ex US 1997-963457 19971103, US 1998-199132 19981124
FDT US 5998820 A Div ex US 5872032
PRAI US 1997-963457 19971103; US 1998-199132 19981124
AB US 5998820 A UPAB: 20000215
NOVELTY - A storage capacitor (305) for storing electrical charge has its plates coupled to substrate biasing voltage Vss (375). A bipolar transistor for amplifying electric charge stored on the capacitor has its base (420) functioning as source of **MOS**-transistor, collector (410) coupled to Vss, emitter (425) coupled to **bit line** control Vbit (320).
DETAILED DESCRIPTION - An n-**MOS** transistor has its gate (460) coupled to a **word line** control Vword (325) to activate and deactivate the transistor and drain (435) to a plate of the capacitor (305). The gate of n-**MOS** transistor is formed by patterning an insulating material to form gate oxide (440) on substrate between drain and source. A **polysilicon** gate is formed above the channel. Implantation of n-type material forms base and implantation of p-type material forms emitter above the base. The collector is formed by diffusing bulk material to form p-well region.
USE - For **DRAM** cells with charge amplification.
ADVANTAGE - **DRAM** cell structures provides charge amplification and a fast write operation. Also the implantation to form base with high energy and large angle provides large current gain.
DESCRIPTION OF DRAWING(S) - The figure shows the cross-sectional diagram of the **DRAM** cell.
Storage capacitor 305
Bit line control 320
Word line control 325
Substrate biasing voltage 375
Collector 410
Base 420
Emitter 425
Drain 435

Gate oxide 440
Gate 460
Dwg.4/8

L62 ANSWER 3 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 1999-625378 [54] WPIX
DNN N1999-462119
TI **Dynamic random** access **memory** structure - determines potential of second **bit line** according to first **bit line**'s potential stored in charge storage electrode.
DC U13 U14
PA (CITL) CITIZEN WATCH CO LTD
CYC 1
PI JP 11274321 A 19991008 (199954)* 7p
ADT JP 11274321 A JP 1998-77164 19980325
PRAI JP 1998-77164 19980325
AB JP 11274321 A UPAB: 20000105
NOVELTY - A charge storage electrode, which is made of **polysilicon** , stores the potential of a first **bit line**. The charge storage electrode is provided at one side of a second active region (212). A ground electrode is provided at the other side of the second active region. The potential of a second **bit line** is determined according to the potential of the charge storage electrode. DETAILED DESCRIPTION - A read **word line** (214) forms a **MOS** on a first active region (206). A write **word line** (216) forms a **MOS** on a second active region (212). The read **word line** and write **word line** are parallel to each other.

USE - None given.

ADVANTAGE - Reduces field area through selective diffusion in active region, and secures memory capacity. DESCRIPTION OF DRAWING(S) - The figure shows the explanatory drawing of the pattern layout of a **DRAM**. (206) First active region; (212) Second active region; (214) Read **word line**; (216) Write **word line**.
Dwg.1/5

L62 ANSWER 4 OF 9 WPIX (C) 2002 THOMSON DERWENT
AN 1994-361590 [45] WPIX
DNN N1994-283464
TI **Metal oxide semiconductor** transistor manufacture method using **silicon** on insulator technology - makes film thickness of source, drain and channel region separately to raise characteristic of SOI **MOS**.
DC U13 U14
PA (SONY) SONY CORP
CYC 1
PI JP 06283683 A 19941007 (199445)* 11p
ADT JP 06283683 A JP 1993-72535 19930330
PRAI JP 1993-72535 19930330
AB JP 06283683 A UPAB: 19950102
The semiconductor device consists of a source domain (8), a drain domain (9) and a channel domain (4). The source drain is connected to capacitor (34) realised on insulated film (1). The channel domain is formed over gate oxide film (31).

The gate electrode is formed under the gate oxide film. The film thickness of the source domain, drain domain are different.

USE/ADVANTAGE - Does not need to form **bit line**

pad so problem of patterning **bit line** is removed and,
in **DRAM**, direct connection of **bit line** and
drain can be achieved and capacitance between **bit line**
and **word line** reduced
Dwg.1/14

L62 ANSWER 5 OF 9 JAPIO COPYRIGHT 2002 JPO
AN 1993-182457 JAPIO
TI **DYNAMIC** SEMICONDUCTOR **MEMORY**
IN WATANABE SHIGEYOSHI
PA TOSHIBA CORP, JP (CO 000307)
PI JP 05182457 A 19930723 Heisei
AI JP1991-356766 (JP03356766 Heisei) 19911226
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: P, Sect. No. 1639, Vol. 17, No. 6, P. 165 (19931108)
AB PURPOSE: To provide the **DRAM** having a small cell size almost the some as the size of an SGT and high reliability.
CONSTITUTION: **Word lines** 15 are formed via gate oxide films 14 on a (p) type **silicon** substrate 11 and (n) type diffusion layers 19, 20 are formed in the respective memory cell regions holding the **word lines** 15. **Bit lines** 21 connected to the (n) type diffusion layers 20 are disposed and are connected to the (n) type diffusion layers 19, by which accumulated node electrodes 22 overlapping on the **word lines** 15 coated with oxide films 16, 17 are formed. Grooves 18 are formed on the substrate along the **word lines** 15 in the stacked capacitor structure disposed with plate electrodes 25 via capacitor oxide films 24 on the accumulated node electrodes 22. The (n) type diffusion layers 19 are formed in the side wall parts of the grooves 18 and the accumulated node electrodes 22 are connected by the side wall parts to the (n) type diffusion layers 19.

L62 ANSWER 6 OF 9 JAPIO COPYRIGHT 2002 JPO
AN 1993-029573 JAPIO
TI SEMICONDUCTOR STORAGE DEVICE AND MANUFACTURE THEREOF
IN KOZAI TAKASHI
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 05029573 A 19930205 Heisei
AI JP1991-184298 (JP03184298 Heisei) 19910724
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 1381, Vol. 17, No. 313, P. 17 (19930615)
AB PURPOSE: To improve the degree of integration of the memory cell of a **DRAM** (**dynamic random** access **memory**).
CONSTITUTION: To obtain the memory cell of a **DRAM** in which **bit lines** 23, access transistors 25, and capacitors 34 are arranged in the vertical direction by forming **word lines** 32 and the capacitors 34 after sticking the first **silicon** substrate 21 on which the **bit lines** 23 are formed and the second **silicon** substrate 22 on which the access transistors 25 are formed in vertical types to each other.

L62 ANSWER 7 OF 9 JAPIO COPYRIGHT 2002 JPO
AN 1990-081471 JAPIO
TI **DYNAMIC RANDOM**-ACCESS **MEMORY** DEVICE
IN TOMA KATSUMI
PA VICTOR CO OF JAPAN LTD, JP (CO 000432)
PI JP 02081471 A 19900322 Heisei
AI JP1988-233306 (JP63233306 Heisei) 19880916
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No.

938, Vol. 14, No. 263, P. 33 (19900607)

AB PURPOSE: To considerably increase the capacitance of a memory capacitor and to secure an excellent sensitivity characteristic by a method wherein a groove having a cross-sectional shape nearly equal to the base of a switching transistor is formed under its face in a substrate, a memory capacitor is formed by filling **polysilicon** via an insulating film formed on an inner wall of this groove and the **polysilicon** is in ohmic contact with the switching transistor.
CONSTITUTION: A groove 44 having an area nearly equal to that of a MOSFET 42 is formed in a **silicon** substrate 41; a nitride film 51 is deposited on an inner wall of the groove 44; after that, **polysilicon** 52 is deposited inside the groove 44; thereby, a memory capacitor is formed. Then, the surface of a processed P-type **silicon** substrate 41 is oxidized thermally; an insulating film 43 is formed. Then, a contact hole 53 is formed in one part of the insulating film 43 in such a way that the **polysilicon** 52 is exposed; a drain 46, a channel 48 and a source 47 are formed. Then, a gate oxide film 49 is formed; after that, a gate electrode 50 is formed. Then, an insulating film 56 is formed; after that, a contact hole is formed; a **word line** 55 and a **bit line** 54 are in ohmic contact individually with the gate electrode 50 and the drain 46; this device is completed.

L62 ANSWER 8 OF 9 JAPIO COPYRIGHT 2002 JPO
AN 1982-069773 JAPIO
TI MANUFACTURE OF SEMICONDUCTOR MEMORY UNIT
IN DENDA MASAHIKO; HARADA KOUJI; NAGASAWA KOICHI; ABE HARUHIKO; KONO YOSHIO
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 57069773 A 19820428 Showa
AI JP1980-145489 (JP55145489 Showa) 19801016
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 123, Vol. 6, No. 1471, P. 60 (19820806)
AB PURPOSE: To enhance density of integration and to obtain a **dynamic random** access **memory** unit contriving enlargement of capacity by a method wherein respective parts of the unit are disposed solidly.
CONSTITUTION: An N+ type diffusion layer 13 is formed selectively on a P+ type **silicon** semiconductor substrate 11, and after a P type semiconductor vapor growth layer 14 is formed, a part of the vapor growth layer 14 is oxidized selectively to form an oxide film 12. Then a part of the oxide film 12 is removed selectively by photo lithography to expose the side part of the removed vapor growth layer 14 and the N+ type diffusion region 13, a gate insulating film 19 is formed on respective exposed parts, and moreover a transfer gate electrode 15 to be connected to a **word line** 18 and a conductive layer 16 to be connected to a **bit line** 17 are formed. The capacitor to be constituted by the semiconductor substrate 11 and the N+ type diffusion region 13 can be integrated solidly, and density of integration is enhanced.

L62 ANSWER 9 OF 9 JAPIO COPYRIGHT 2002 JPO
AN 1982-069772 JAPIO
TI SEMICONDUCTOR MEMORY UNIT
IN NAGASAWA KOICHI; HARADA HIROJI; DENDA MASAHIKO; ABE HARUHIKO; KONO YOSHIO
PA MITSUBISHI ELECTRIC CORP, JP (CO 000601)
PI JP 57069772 A 19820428 Showa
AI JP1980-145481 (JP55145481 Showa) 19801016
SO PATENT ABSTRACTS OF JAPAN, Unexamined Applications, Section: E, Sect. No. 123, Vol. 6, No. 1471, P. 59 (19820806)

AB PURPOSE: To enhance density of integration and to obtain a **dynamic random** access **memory** unit contriving enlargement of capacity thereof by a method wherein respecitve parts of the unit are disposed solidly.
CONSTITUTION: A field insulating film 12 and an n+ type diffusion region 13 are formed on a p type **silicon** semiconductor substrate 11. The n+ type diffusion region 13 constitutes a capacitor between the semiconductor substrate 11. A p+ type vapor growth layer 14 is formed selectively on the n+ type diffusion region 13, and moreover a transfer gate electrode 15 consisting of polycrystalline **silicon** to be connected to a **word line** 18 through a gate insulating film 19 is formed, and an n+ type vapor growth layer 16 to be connected to a **bit line** 17 is formed on the p+ type vapor growth layer 14. Because the transfer transistor being length of the gate electrode thereof decided by thickness of polycrystalline **silicon** is constituted in the vertical direction, and the transistor and the capacitor are integrated solidly, density of integration is enhanced.

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  File 315:ChemEng & Biotec Abs  1970-2002/Jun
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Set	Items	Description
S1	2992360	(METAL()OXIDE()SEMICONDUCTOR? ?) OR VMOS? ? OR MOS? ? OR N-MOS? ? OR PMOS? ? OR MOSFET? ?
S2	12175	(EDRAM? ? OR CDRAM? ? OR (EMBEDDED OR ENHANCE?)()(DRAM? ?) OR EMBEDDEDDRAM? ? OR DYNAMIC(2N)MEMOR?)
S3	229678	(ENHANCE? OR EMEBBED)(W)DYNAMIC()RANDOM()ACCESS()MEMOR? OR EDRAM? ? OR CDRAM? ? OR ((CACHE OR E OR C)()(DRAM? ? OR RANDOM(2N)MEMOR?)) OR CACHEDRAM? ? OR (EMBEDDED OR ENHANCE()DYNAMIC(2N)MEMOR?)
S4	32270	DRAM? ? OR D()RAM? ? OR DYNAMIC()RAM? ? OR DYNAMICRAM? OR (D OR DYNAMIC?)()(RANDOM (2N)MEMOR?)
S5	800787	EMBED???? OR IMBED???? OR ENTRENCH? OR FASTEN? OR INFIX?? OR INGRAIN? OR IMPLANT?
S6	240855	VERTICUL? OR PERPENDICULAR? OR UPRIGHT
S7	22004	S1 AND (S2 OR S3)
S8	1769	S7 AND S4
S9	1299785	POLYSILICON OR SILICON OR HEXSIL OR HGH()600 OR KDB()20OR OR METASILICON()325A OR POLYSILICON OR SICOMILL()4C()P OR SICOMILL OR SILGRAIN SILICON OR SILSO
S10	35	S8 AND (WORDLINE? ? OR WORD()LINE? ?) AND (BITLINE? ? OR BIT()LINE? ?)
S11	1299791	POLYSILICON OR SILICON OR HEXSIL OR HGH()600 OR KDB()20OR OR METASILICON()325A OR POLYSILICON OR SICOMILL()4C()P OR SICOMILL OR SILGRAIN OR SILICON OR SILSO
S12	35	S10
S13	27	RD (unique items)
S14	437	S8 AND S11
S15	1	S14 AND S6
S16	0	S15 NOT S12
S17	166	S14 AND GATE? ?
S18	122	RD (unique items)
S19	118	S18 NOT S12
S20	26	S19 AND (ARRAY OR ARRANG??? OR ORDER OR ORGANIZ? OR RANG??? OR SORT??? OR SYSTEMATIZE)
S21	33	S19 AND (BODY OR BUNCH?? OR BUNDLE OR CLUMP OR CLUSTER OR COLLECTION OR GROUP)
S22	56	S20 OR S21
S23	5	S22 AND S5
S24	0	S19 AND (BITLINE OR BIT()LINE? ?) AND (WORDLINE? ? OR WORD()LINE? ?)
S25	7	S19 AND (BITLINE OR BIT()LINE? ?)
S26	2	S19 AND (WORDLINE? ? OR WORD()LINE? ?)
S27	8	(S25 OR S26) NOT (S12 OR S15 OR S23)
S28	2	S8 AND S6
S29	1	S28 NOT (S12 OR S15 OR S23 OR S25 OR S26)
S30	437	S8 AND S11
S31	57	S30 AND S5
S32	49	RD (unique items)
S33	43	S32 NOT (S12 OR S15 OR S23 OR S25 OR S26 OR S28)

13/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

6747707 INSPEC Abstract Number: B2000-12-1265D-017, C2000-12-5320G-004
Title: Process integration trends for **embedded DRAM**
Author(s): Takato, H.; Koike, H.; Yoshida, T.; Ishiuchi, H.
Author Affiliation: Microelectron. Eng. Lab., Toshiba Corp., Yokohama, Japan
Conference Title: ULSI Process Integration. Proceedings of the First International Symposium (Electrochemical Society Proceedings Vol.99-18) p.107-19
Editor(s): Claeys, C.L.; Iwai, H.; Bronner, G.; Fair, R.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1999 Country of Publication: USA xiii+386 pp.
ISBN: 1 56677 241 9 Material Identity Number: XX-2000-00269
Conference Title: Proceedings of ULSI Process Integration
Conference Sponsor: Electrochem. Soc
Conference Date: 17-22 Oct. 1999 Conference Location: Honolulu, HI, USA
Language: English
Abstract: Issues and development trends with respect to **embedded DRAM** (**eDRAM**) technology are reviewed by referring to real implementations for 0.5 mu m, 0.35 mu m and 0.25 mu m generations. Chip performance has been progressively improved throughout the development of 0.5 mu m, 0.35 mu m and 0.25 mu m **eDRAM**. However, the number of process steps has increased compared to that for commodity **DRAM**. To avoid this problem and achieve the highest possible device performance, future directions for **embedded DRAM** technologies, including **MOSFET** structure, memory cells, process cost and performance, are also discussed. For the **MOSFET** structure, the logic-based **MOSFET** process offers more advantages than the **DRAM**-based one for future **eDRAM** generations. For memory cell structure, the trench cell is expected to be more useful for future **eDRAM** compared to the stacked cell. In order to combine the trench cell and logic based **MOSFET** process, a new **embedded DRAM** technology is proposed. This process technology provides full process compatibility with high performance logic and a minimum number of process steps, resulting in low process cost and short TAT (turnaround time). A **DRAM** array macro has been fabricated using this technology with Co salicide, dual work function gate and aluminum **bit-line** processes, and excellent **DRAM** retention characteristics have been confirmed using a negative **word-line** bias scheme.
Subfile: B C

13/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

6737400 INSPEC Abstract Number: B2000-12-0520F-010
Title: Plasma enhanced chemical vapor deposition Si-rich silicon oxynitride films for advanced self-aligned contact oxide etching in sub-0.25 mu m ultralarge scale integration technology and beyond
Author(s): Jeong-Ho Kim; Jae-Seon Yu; Ja-Chun Ku; Choon-Kun Ryu; Su-Jin Oh; Si-Bum Kim; Jin-Woong Kim; Jeong-Mo Hwang; Su-Youb Lee; Kouichiro, I.
Author Affiliation: Semicond. Adv. Res. Div., Hyundai Electron. Ind. Co.

Ltd., South Korea
Journal: Journal of Vacuum Science & Technology A (Vacuum, Surfaces, and Films) Conference Title: J. Vac. Sci. Technol. A, Vac. Surf. Films (USA) vol.18, no.4, pt.1-2 p.1401-10
Publisher: AIP for American Vacuum Soc,
Publication Date: July-Aug. 2000 Country of Publication: USA
CODEN: JVTAD6 ISSN: 0734-2101
SICI: 0734-2101(200007/08)18:4:1/2L.1401:PECV;1-2
Material Identity Number: D746-2000-005
U.S. Copyright Clearance Center Code: 0734-2101/2000/18(4)/1401(10)/$15.0 0
Conference Title: 46th National Symposium of the American Vacuum Society. Vacuum, Surfaces, and Films
Conference Date: 25-29 Oct. 1999 Conference Location: Seattle, WA, USA
Language: English
Abstract: We intentionally introduced excessive Si during the SiO/sub x/N/sub y/ film deposition in order to increase the etch selectivity-to-SiO/sub x/N/sub y/ for advanced self-aligned contact (SAC) etching in sub-0.25 mu m ultralarge scale integration devices. The SiO/sub x/N/sub y/ layer was deposited at a conventional plasma enhanced chemical vapor deposition chamber by using a mixture of SiH/sub 4/, NH/sub 3/, N/sub 2/O, and He. The gas mixing ratio was optimized to get the best etch selectivity and low leakage current. The best result was obtained at 10% Si-SiO/sub x/N/sub y/. In order to employ SiO/sub x/N/sub y/ film as an insulator as well as a SAC barrier, the leakage current of SiO/sub x/N/sub y/ film was evaluated so that SiO/sub x/N/sub y/ may have the low leakage current characteristics. The leakage current of 10% Si-SiO/sub x/N/sub y/ film was 7*10/sup -9/ A/cm/sup 2/. Besides, the Si-rich SiO/sub x/N/sub y/ layer excellently played the roles of antireflection coating for **word line** and **bit line** photoresist patterning and sidewall spacer to build a **metal-oxide-semiconductor** transistor as well as a SAC oxide etch barrier. The contact oxide etching with the Si-rich SiO/sub x/N/sub y/ film was done using C/sub 4/F/sub 8//CH/sub 2/F/sub 2//Ar in a dipole ring magnet plasma. As the C/sub 4/F/sub 8/ flow rate increases, the oxide etching selectivity-to-SiO/sub x/N/sub y/ increases but etch stop tends to happen. Our optimized contact oxide etch process showed the high selectivity to SiO/sub x/N/sub y/ larger than 25 and a wide process window (>or=5 sccm) for the C/sub 4/F/sub 8/ flow rate. When the Si-rich SiO/sub x/N/sub y/ SAC process was applied to a gigabit **dynamic random** access **memory** of cell array, there was no electrical short failure between conductive layers.
Subfile: B

13/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

5802161 INSPEC Abstract Number: B9802-2570D-029
Title: Low temperature metal-based cell integration technology for gigabit and **embedded DRAMs**
Author(s): Yoshida, M.; Kumauchi, T.; Kawakita, K.; Ohashi, N.; Enomoto, H.; Umezawa, T.; Yamamoto, N.; Asano, I.; Tadaki, Y.
Author Affiliation: Device Dev. Center, Hitachi Ltd., Tokyo, Japan
Conference Title: International Electron Devices Meeting 1997. IEDM Technical Digest (Cat. No.97CH36103) p.41-4
Publisher: IEEE, New York, NY, USA
Publication Date: 1997 Country of Publication: USA 944 pp.

ISBN: 0 7803 4100 7 Material Identity Number: XX97-03283
U.S. Copyright Clearance Center Code: 0 7803 4100 7/97/$10.00
Conference Title: International Electron Devices Meeting. IEDM Technical Digest
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 7-10 Dec. 1997 Conference Location: Washington, DC, USA
Language: English
Abstract: An advanced memory cell structure with poly/metal **word lines** and metal **bit lines** is proposed. The thermal processes are carefully designed for the metal-based cell to be consistent with narrow gap filling, wet cleaning, planarity, and the contact process. The extremely low temperature process also helps suppress the short channel effect of the **MOS** transistors. The fully self-aligned contact and via-hole technology provides the minimum memory cell area. This technology is promising for future gigabit **DRAMs** and **embedded DRAMs**.

Subfile: B

13/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

5241835 INSPEC Abstract Number: B9605-1265D-056, C9605-5320G-039
Title: Giga-bit **DRAM** cells with low capacitance and low resistance **bit-lines** on buried **MOSFETs** and capacitors by using bonded SOI technology-reversed stacked capacitor (RSTC) cell
Author(s): Nakamura, S.; Horie, H.; Asano, K.; Nara, Y.; Fukano, T.; Sasaki, N.
Author Affiliation: Fujitsu Labs. Ltd., Atsugi, Japan
Conference Title: International Electron Devices Meeting. Technical Digest (Cat. No.95CH35810) p.889-92
Publisher: IEEE, New York, NY, USA
Publication Date: 1995 Country of Publication: USA 1026 pp.
ISBN: 0 7803 2700 4 Material Identity Number: XX95-02847
U.S. Copyright Clearance Center Code: 0 7803 2700 4/96/$4.00
Conference Title: Proceedings of International Electron Devices Meeting
Conference Sponsor: IEEE Electron. Devices Soc
Conference Date: 10-13 Dec. 1995 Conference Location: Washington, DC, USA
Language: English
Abstract: This paper describes a reversed-stacked-capacitor (RSTC) cell for Giga-bit **DRAMs**, where a storage capacitor and a **MOSFET** are reversed by using chemical-mechanical-polishing (CMP) and bonded-SOI technology. The virtual flat surface at the bottom of the **MOSFET** is made into a real surface by polishing. The **bit-lines** and metal wirings are realized on the flat surface with low-aspect-ratio contact holes throughout the whole chip. This cell structure is suitable for not only Giga-bit **DRAMs** but also **embedded DRAMs**. A test memory array is fabricated with a 64 Mbit **DRAM** design rule. Both capacitance and resistance of **bit-lines** decreased by a factor of two with this RSTC cell compared to the conventional shielded-**bit-line** STC cells. The **bit-lines** are placed far from **word-lines** and cell-capacitors. The **bit-lines** are made of low resistivity materials after all the high-temperature processes have been finished.
Subfile: B C

13/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

03854525 INSPEC Abstract Number: B91023599
Title: Buried **bit-line** cell for 64 Mb **DRAMs**
Author(s): Kohyama, Y.; Yamamoto, T.; Sudo, A.; Watanabe, T.; Tanaka, T.
Author Affiliation: Toshiba Corp., Kawasaki, Japan
Conference Title: 1990 Symposium on VLSI Technology. Digest of Technical Papers (Cat. No.90CH2874-6) p.17-18
Publisher: IEEE, New York, NY, USA
Publication Date: 1990 Country of Publication: USA xvii+143 pp.
U.S. Copyright Clearance Center Code: CH2874-6/90/0000-0017$01.00
Conference Sponsor: IEEE; Japan Soc. Appl. Phys
Conference Date: 4-7 June 1990 Conference Location: Honolulu, HI, USA
Language: English
Abstract: The authors propose a buried **bit-line** (BBL) stacked capacitor cell structure for high-density **dynamic random** access **memories** (**DRAMs**). The cell area can be reduced to as small as 8.7F/sup 2/, where F is the lithographic feature size. A 2.25- mu m/sup 2/ cell area is achieved using a 0.51- mu m feature size. A 1.4- mu m/sup 2/ cell area is attainable using a 0.4- mu m feature size. The memory-cell vertical size (2F) includes a line and space for a trench isolation pattern in which the buried **bit-line** is formed. The horizontal size (4F+a) includes two **word-line** line and space pairs and a **word-line** to **bit-line** contact alignment tolerance denoted by a. A storage node contact is self-aligned to the **word-line** . Since the a is considered to be less than F/2, a cell area of less than 9F/sup 2/ is realized. If the **bit-line** contact is also self-aligned to the **word-line**, an 8F/sup 2/ cell area can in theory be realized.
Subfile: B

13/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

02322346 INSPEC Abstract Number: B84051247, C84044478
Title: A sub 100 ns 256K **DRAM** in CMOS III technology
Author(s): Kung, R.I.; Mohsen, A.M.; Schutz, J.D.; Madland, P.D.; Webb, C.C.; Handy, E.R.; Simonsen, C.J.; Guo, R.T.; Yu, K.K.; Chou, S.
Author Affiliation: Intel Corp., Aloha, OR, USA
Conference Title: 1984 IEEE International Solid-State Circuits Conference. Digest of Technical Papers p.278-9, 354
Publisher: Lewis Winner, Coral Gables, FL, USA
Publication Date: 1984 Country of Publication: USA 384 pp.
U.S. Copyright Clearance Center Code: 0193-6530/84/0000-0278$01.00
Conference Sponsor: IEEE; Univ. Pennsylvania
Conference Date: 22-24 Feb. 1984 Conference Location: San Francisco, CA, USA
Language: English
Abstract: The **DRAM** utilizes a p-channel array, signal sensing, and clocked CMOS circuits. The 256K memory array is organized in 8 identical blocks with a folded metal **bit-line** and poly **word-line** configuration. The **word-line** delay is reduced by the

use of dual row decoders and drivers. Each of the 8 memory blocks is further divided into two halves by the sense amplifiers. A multiplexed sense amplifier is used to halve the **bit-line** length, thus improving the **bit-line** -to-cell capacitance ratio. Signal sensing is accomplished by a clocked p-channel latch which is totally isolated from its **bit lines** during sensing. A p-channel one-transistor cell **embedded** in an n-well biased at V/sub DD/ potential is used in the memory array. The n-well substrate reverse-biased junction acts as an effective minority carrier barrier to reduce soft errors induced by alpha particles, improve the array refresh characteristics and isolate the memory cells from substrate noise injected by the peripheral circuits.
Subfile: B C

13/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

01879629 INSPEC Abstract Number: B82035981, C82026925
Title: Characterization of **MoSi**/sub 2/-gate buried channel **MOSFETs** for a 256K-bit **dynamic RAM**
Author(s): Tanaka, T.; Ishiuchi, H.; Takeuchi, Y.; Ishikawa, M.; Mochizuki, T.; Ozawa, O.
Author Affiliation: Semiconductor Device Engng. Lab., Toshiba Corp., Horikawacho, Saiwaiku, Kawasaki-city, Kanagawa, Japan
Conference Title: International Electron Devices Meeting p.659-62
Publisher: IEEE, New York, NY, USA
Publication Date: 1981 Country of Publication: USA 711 pp.
Conference Sponsor: IEEE
Conference Date: 7-9 Dec. 1981 Conference Location: Washington, DC, USA
Language: English
Abstract: Basic characteristics of **MoSi**/sub 2/-gate **MOSFETs** have been studied, placing main emphasis on implementation of 256K-bit **dynamic RAM**. Both simulation and experiments suggest that the **MoSi**/sub 2/-gate **MOSFET** exhibit good controllability for threshold voltage, low leakage current level in the subthreshold region and stable threshold voltage during BT-stress, which allows the design of a 256K-bit **dynamic memory**. **MoSi**/sub 2/ **word line**/metal **bit line** cells and **MoSi**/sub 2/-gate **MOSFETs** in the peripheral circuits, thus, appears to be the **most** appropriate configuration for a 256K-bit RAM.
Subfile: B C

13/3,AB/8 (Item 8 from file: 2)
DIALOG(R)File 2:INSPEC

01558368 INSPEC Abstract Number: B80039990
Title: A one-device memory cell using a single layer of polysilicon and a self-registering metal-to-polysilicon contact
Author(s): Rideout, V.L.; Cramer, A.; Walker, J.J.
Author Affiliation: IBM Thomas J. Watson Res. Centre, Yorktown Heights, NY, USA
Journal: IBM Journal of Research and Development vol.24, no.3 p. 339-47
Publication Date: May 1980 Country of Publication: USA

CODEN: IBMJAE ISSN: 0018-8646
Language: English
Abstract: The fabrication and operation of a novel one-device **dynamic memory** cell are described. Like the conventional double overlapping polysilicon cell, the new memory cell has a diffused **bit line** and a metal **word line** , uses five basic masking operations, and provides essentially equivalent cell area for the same lithographic feature size. Unlike the double polysilicon cell, however, the new cell uses a single layer of polysilicon to provide a more planar surface topography, and a self-registering metal-to-polysilicon contact to provide a small cell area. An essential aspect of the fabrication method of the self-registered contact cell is the use of two lithographic masking operations that define two patterns in a single polysilicon layer, the **MOSFET** gate electrode and the **MOS** capacitor electrode. The self-registering contact also facilitates a powerful polysilicon wiring technique that is applicable to the access circuits located peripherally to the array of memory cells.
Subfile: B

13/3,AB/9 (Item 9 from file: 2)
DIALOG(R)File 2:INSPEC

01422567 INSPEC Abstract Number: B79047285, C79030068
Title: One-device cells for **dynamic random**-access **memories**: a tutorial
Author(s): Rideout, V.L.
Author Affiliation: IBM Thomas J. Watson Res. Center, Yorktown Heights, NY, USA
Journal: IEEE Transactions on Electron Devices vol.ED26, no.6 p. 839-52
Publication Date: June 1979 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
Language: English
Abstract: The evolutionary development of one-device cells for **dynamic random**-access **memory** (RAM) integrated circuits is described. From an examination of the areal layout (planar top view) and the cross section (vertical topography), various memory cells are compared in a systematic manner. Structural features such as contact via formation, **bit-line** and **word-line** pitch, metal step coverage, and cell placement along the **bit line** are also considered. Some new **dynamic RAM** cell concepts such as doubly doped storage capacitors, self-registering contacts, and **VMOS** FET's are discussed. From an examination of commercially available **dynamic RAM** chips, a basic lithographic groundrule was determined.
Subfile: B C

13/3,AB/10 (Item 10 from file: 2)
DIALOG(R)File 2:INSPEC

01400567 INSPEC Abstract Number: B79038431, C79027171
Title: Double polysilicon **dynamic memory** cell with polysilicon **bit line**
Author(s): Rideout, V.L.
Author Affiliation: IBM Corp., Armonk, NY, USA
Journal: IBM Technical Disclosure Bulletin vol.21, no.9 p.3828-31

Publication Date: Feb. 1979 Country of Publication: USA
CODEN: IBMTAA ISSN: 0018-8689
Language: English
Abstract: The overlapping double polysilicon **dynamic memory** cell is the **most** popular cell for 16 and 64 kb **dynamic random**-access **memories** . The cell, which requires five basic lithographic masking steps, provides a diffused N+ **bit line** and a metal **word line** connected to two polysilicon gates.
Subfile: B C

13/3,AB/11 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

06057013
E.I. No: EIP02216955097
Title: A capacitor-less 1T-**DRAM** cell
Author: Okhonin, S.; Nagoga, M.; Sallese, J.M.; Fazan, P.
Corporate Source: LEG Swiss Federal Inst. of Technol., CH-1015 Lausanne, Switzerland
Source: IEEE Electron Device Letters v 23 n 2 February 2002. p 85-87
Publication Year: 2002
CODEN: EDLEDZ ISSN: 0741-3106
Language: English
Abstract: A simple true 1 transistor **dynamic random** access **memory** (**DRAM**) cell concept is proposed for the first time, using the body charging of partially-depleted SOI devices to store the logic "1" or "0" binary states. This cell is two times smaller in area than the conventional 8F**2 1T/1C **DRAM** cell and the process of its manufacturing does not require the storage capacitor fabrication steps. This concept will allow the manufacture of simple low cost **DRAM** and **embedded DRAM** chips for 100 and sub-100 nm generations. 12 Refs.

13/3,AB/12 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05508515
E.I. No: EIP00035094188
Title: Perspectives on giga-bit scaled **DRAM** technology generation
Author: Kim, Kinam
Corporate Source: Samsung Electronics Co, Kyungki-Do, South Korea
Source: Microelectronics and Reliability v 40 n 2 2000. p 191-206
Publication Year: 2000
CODEN: MCRLAS ISSN: 0026-2714
Language: English
Abstract: As the density of **DRAM** approaches giga-bit scaled **DRAM**, many critical challenges emerge from its small cell size. The **most** critical obstacles are insufficient cell capacitance and large leakage current at storage junction. Besides, variation of threshold voltage of memory cell transistor and the increased delay of **word line** and **bit line** come up to limit performance of device.
In this paper, the critical issues in giga-bit technology are reviewed and appropriate approaches to overcome these issues are discussed based on the technology generation. The discussions are mainly focused on the key technologies: memory cell capacitor technology, memory cell transistor

technology, **word line** and **bit line** technology,
memory cell connection technology and metallization technology. Down to the 0.10 mu m technology generation, we can specifically define the challenges for each technology generation and can find the ways to overcome these obstacles with proper technology migrations based on the current Capaciton-Over-**bit line** cell structure. The technology migration will move toward Ta//2O//5 capacitor, modified memory cell transistor, W-gate, W-**bit line** and self-aligned landing pad technology in cost-effective ways. Beyond the 0.10 mu m technology generation, breakthrough technology seems to be indispensable. The breakthrough technology should happen in memory cell concept, memory cell structure and integration technology. (Author abstract) 31 Refs.

13/3,AB/13 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04624882
E.I. No: EIP97023516176
Title: 0.23 mu m**2 double self-aligned contact cell for gigabit **DRAMs** with a Ge-added vertical epitaxial Si pad
Author: Koga, H.; Kasai, N.; Hada, H.; Tatsumi, T.; Mori, H.; Iwao, S.; Saino, K.; Yamaguchi, H.; Nakajima, K.; Yamada, Y.; Tokunaga, K.; Hirasawa, S.; Yoshida, K.; Nishizawa, A.; Hashimoto, T.; et al
Corporate Source: NEC Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1996 IEEE International Electron Devices Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19961208-19961211
E.I. Conference No.: 46059
Source: Technical Digest - International Electron Devices Meeting 1996. IEEE, Piscataway, NJ, USA,96CH35961. p 589-592
Publication Year: 1996
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: A new stacked capacitor memory cell with folded **bit-line** arrangement has been developed using a double self-aligned contact technology. By using a combination of a vertical epitaxial growth Si pad and Si//3N//4 caps as etch stop layers on both the **bit-lines** and **word-lines**, the cell area using 0.15 mu m design rule can be reduced to 0.23 mu m**2 with 0.1 mu m alignment tolerance. Through addition of germanium (Ge) to the Si pad, the controllability of epitaxially grown Si pad features can be improved, resulting in an increase in the growth rate ratio of perpendicular to lateral directions by a factor of 4 and a decrease in resistance of the epi pad from 5k Omega to 1k Omega . (Author abstract) 6 Refs.

13/3,AB/14 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04001605
E.I. No: EIP94122451194
Title: Vertical Phi -shape transistor (V Phi T) cell for 1Gbit **DRAM** and beyond
Author: Maeda, S.; Maegawa, S.; Ipposhi, T.; Nishimura, H.; Kuriyama, H.; Tanina, O.; Inoue, Y.; Nishimura, T.; Tsubouchi, N.

Corporate Source: ULSI Lab Mitsubishi Electric Corp, Hyogo, Jpn
Conference Title: Proceedings of the 1994 Symposium on VLSI Technology
Conference Location: Honolulu, HI, USA Conference Date: 19940607-19940609
E.I. Conference No.: 21361
Source: Digest of Technical Papers - Symposium on VLSI Technology 1994. IEEE, Piscataway, NJ, USA,94CH3433-0. p 133-134
Publication Year: 1994
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: We propose a Vertical Phi -shape Transistor (V Phi T) cell for 1Gbit **DRAM** and beyond. The V Phi T is a vertical **MOSFET** whose gate surrounds its channel region like a Greek alphabet Phi . It is built by penetration of the gate electrode (equals **word line**) which has been formed beforehand. Application of the V Phi T for **DRAM** cell brings about cell size reduction to 50% and process simplification of about 10% at least, mainly because its **bit line** contact and the V Phi T are vertically aligned and storage node contact is eliminated. We have indicated that the V Phi T is an interesting candidate for the gigabit **DRAM** in view of size, cost and performance. (Author abstract) 12 Refs.

13/3,AB/15 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

03894125
E.I. No: EIP94071336921
Title: Design rule relaxation approach for high-density **DRAMs**
Author: Saeki, Takanori; Kakehashi, Eiichiro; Mori, Hidemitu; Koga, Hiroki; Noda, Kenji; Fujita, Mamoru; Sugawara, Hiroshi; Nagata, Kyoichi; Nishimoto, Shozo; Murotani, Tatsunori
Corporate Source: NEC Corp, Sagamihara-shi, Jpn
Source: IEICE Transactions on Electronics v E77-C n 3 Mar 1994. p 406-415
Publication Year: 1994
CODEN: IELEEJ ISSN: 0916-8524
Language: English
Abstract: A design rule relaxation approach is one of the **most** important requirements for high density **DRAMs**. The approach relaxes the design rule of a element in comparison with the memory cell size and provides high density **DRAMs** with the minimum development of a scaled-down **MOS** structure and a fine patterning lithography process. This paper describes two design rule relaxation approaches, a close-packed folded (CPF) **bit-line** cell array layout and a Boosted Dual **Word-Line** scheme. The CPF cell array provides 1.26 times wider active area pitch and maximum 1.5 times wider isolation width. The Boosted Dual **Word-Line** scheme provides 2**n times wider 1st Al pitch on memory cell array, double **word-line** driver pitch and 1.5 times larger design rule for 1st Al and contacts under 1st Al. Especially wide design rule of the Boosted Dual **Word-Line** scheme provides several times depth of focus (DOF) for 1st Al wiring which gives several times higher storage node and larger capacitance for capacitor over **bit-line** (COB) stacked capacitor cells. These approaches are successfully implemented in a 4 Mb **DRAM** test chip with a 0.9 multiplied by 1.8 mu m**2 memory cell. (Author abstract) 14 Refs.

13/3,AB/16 (Item 6 from file: 8)

DIALOG(R)File 8:Ei Compendex(R)

03394565
E.I. Monthly No: EI9203031448
Title: A 33-ns 64-Mb **DRAM**.
Author: Oowaki, Yukihito; Tsuchida, Kenji; Watanabe, Yohji; Takashima, Daisaburo; Ohta, Masako; Nakano, Hiroaki; Watanabe, Shigeyoshi; Nitayama, Akihiro; Horiguchi, Fumio; Ohuchi, Kazunori; Masuoka, Fujio
Corporate Source: Toshiba Corp, Saiwai-ku, Kawasaki, Japan
Source: IEEE Journal of Solid-State Circuits v 26 n 11 Nov 1991 p 1498-1505
Publication Year: 1991
CODEN: IJSCBC ISSN: 0018-9200
Language: English
Abstract: A 64-Mb CMOS **dynamic RAM** (**DRAM**) measuring 176.4 mm**2 has been fabricated using a 0.4- mu m N-substrate triple-well CMOS, double-poly, double-polycide, double-metal process technology. Asymmetrical stacked-trench capacitor (AST) cells, 0.9 mu m multiplied by 1.7 mu m each, are laid out in a **PMOS** centered interdigitated twisted **bit-line** (PCITBL) scheme that achieves both low noise and high packing density. Three circuit techniques were developed to meet high-speed requirements. Using the preboosted **word-line** drive-line technique, a bypassed sense-amplifier drive-line scheme, and a quasi-static data transfer technique, a typical RAS access time of 33 ns and a typical column address access time of 15 ns have been achieved. 9 Refs.

13/3,AB/17 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

02518758
E.I. Monthly No: EI8802012200
Title: 4-MBIT **DRAM** WITH FOLDED-**BIT-LINE** ADAPTIVE SIDEWALL-ISOLATED CAPACITOR (FASIC) CELL.
Author: Mashiko, Koichiro; Nagatomo, Masao; Arimoto, Kazutami; Matsuda, Yoshio; Furutani, Kiyohiro; Matsukawa, Takayuki; Yamada, Michihiro; Yoshihara, Tsutomu; Nakano, Takao
Corporate Source: Mitsubishi Electric Corp, Jpn
Source: IEEE Journal of Solid-State Circuits v SC-22 n 5 Oct 1987 p 643-650
Publication Year: 1987
CODEN: IJSCBC ISSN: 0018-9200
Language: ENGLISH
Abstract: A 5-V 4-Mb word X 1-b/1-Mb word X 4-b **dynamic RAM** with a static column mode and fast page mode has been built in a 0. 8 MU m twin-tub CMOS technology with single-metal, two-polycide, and single poly-Si interconnections. It uses an innovative folded-**bit-line** adaptive sidewall-isolated capacitor (FASIC) cell that measures 10. 9 MU m**2 and requires only a 2 MU m trench to obtain a storage capacitor of 50 fF with 10 nm SiO//2 equivalent dielectric film. A shared-**PMOS** sense-amplifier architecture used in this **DRAM** provides a low power consumption, small C//B-to-C//S capacitance ratio, and accurate reference level for the nonboosted **word-line** scheme with little area penalty. These concepts have allowed the **DRAM** to be housed in the industry standard 300 mil dual-in-line package with performances of 90 ns RAS access time and 30 ns column address access time. 21 refs.

13/3,AB/18 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

08850785 Genuine Article#: 335ZH Number of References: 15
Title: Plasma enhanced chemical vapor deposition Si-rich silicon oxynitride films for advanced self-aligned contact oxide etching in sub-0.25 mu m ultralarge scale integration technology and beyond (ABSTRACT AVAILABLE)
Author(s): Kim JH (REPRINT) ; Yu JS; Ku JC; Ryu CK; Oh SJ; Kim SB; Kim JW; Hwang JM; Lee SY; Kouichiro I
Corporate Source: HYUNDAI ELECT IND CO LTD,SEMICOND ADV RES DIV, SAN 136-1/INCHON 467701/KYONGKI/SOUTH KOREA/ (REPRINT); TEL KOREA LTD,/YONGIN 449840/KYOUNGKI/SOUTH KOREA/; TOKYO ELECTRON YAMANASHI LTD,/YAMANASHI 407//JAPAN/
Journal: JOURNAL OF VACUUM SCIENCE & TECHNOLOGY A-VACUUM SURFACES AND FILMS , 2000, V18, N4,1 (JUL-AUG), P1401-1410
ISSN: 0734-2101 Publication date: 20000700
Publisher: AMER INST PHYSICS, 2 HUNTINGTON QUADRANGLE, STE 1NO1, MELVILLE, NY 11747-4501
Language: English Document Type: ARTICLE
Abstract: We intentionally introduced excessive Si during the SiOxNy film deposition in order to increase the etch selectivity-to-SiOxNy for advanced self-aligned contact (SAC) etching in sub-0.25 mu m ultralarge scale integration devices. The SiOxNy layer was deposited at a conventional plasma enhanced chemical vapor deposition chamber by using a mixture of SiH4, NH3, N2O, and He. The gas mixing ratio was optimized to get the best etch selectivity and low leakage current. The best result was obtained at 10% Si-SiOxNy. In order to employ SiOxNy film as an insulator as well as a SAC barrier, the leakage current of SiOxNy film was evaluated so that SiOxNy may have the low leakage current characteristics. The leakage current of 10% Si-SiOxNy film was 7 x 10(-9) A/cm(2). Besides, the Si-rich SiOxNy layer excellently played the roles of antireflection coating for **word line** and **bit line** photoresist patterning and sidewall spacer to build a **metal-oxide-semiconductor** transistor as well as a SAC oxide etch barrier. The contact oxide etching with the Si-rich SiOxNy film was done using C4F8/CH2F2/Ar in a dipole ring magnet plasma. As the C4F8 flow rate increases, the oxide etching selectivity-to-SiOxNy increases but etch stop tends to happen. Our optimized contact oxide etch process showed the high selectivity to SiOxNy larger than 25 and a wide process window (greater than or equal to 5 sccm) for the C4F8 flow rate. When the Si-rich SiOxNy SAC process was applied to a gigabit **dynamic random** access **memory** of cell array, there was no electrical short failure between conductive layers. (C) 2000 American Vacuum Society. [S0734-2101(00) 16504-2].

13/3,AB/19 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03162794 JICST ACCESSION NUMBER: 97A0476649 FILE SEGMENT: JICST-E
Circuit Technologies for Memory and Analog LSIs. Folded **Bitline** Architecture for a Gigabit-Scale NAND **DRAM**.
SHIRATAKE S (1); HASEGAWA T (1); NAKANO H (1); OHSAWA T (1); TAKASHIMA D (2); OOWAKI Y (2); WATANABE S (2); OHUCHI K (2)
(1) Toshiba Corp., Yokohama-shi, JPN; (2) Toshiba Corp., Kawasaki-shi, JPN

IEICE Trans Electron(Inst Electron Inf Commun Eng), 1997, VOL.E80-C,NO.4,
PAGE.573-581, FIG.16, REF.7
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: A new memory cell arrangement for a gigabit-scale NAND **DRAM** is proposed. Although the conventional NAND **DRAM** in which memory cells are connected in series realizes the small die size, it faces a crucial array noise problem in the I gigabit generation and beyond because of its inherent noise of the open **bitline** arrangement. By introducing the new cell arrangement to a NAND **DRAM**, the folded **bitline** scheme is realized, resulting in good noise immunity. The basic operation of the proposed folded **bitline** scheme was successfully verified using the 64 kbit test chip. The die size of the proposed NAND **DRAM** with the folded **bitline** scheme (F-NAND **DRAM**) at the 1 Gbit generation is reduced to 63% of that of the conventional 1 Gbit **DRAM** with the folded **bitline** scheme, assuming the **bitlines** and the **wordlines** are fabricated with the same pitch. The new 4/4 **bitline** grouping scheme in which cell data are read out to four neighboring **bitlines** is also introduced to reduce the **bitline**-to-**bitline** coupling noise to half of that of the conventional folded **bitline** scheme. The array noise of the proposed F-NAND **DRAM** with the 4/4 **bitline** grouping scheme at 1 Gbit generation is reduced to 10% of the read-out signal, while that of the conventional NAND **DRAM** with open **bitline** scheme is 29%, and that of the conventional **DRAM** with the folded **bitline** scheme is 22%. (author abst.)

13/3,AB/20 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02987939 JICST ACCESSION NUMBER: 96A0705414 FILE SEGMENT: JICST-E
SOI-**DRAM** Circuit Technologies for Low Power High Speed Multigiga Scale Memories.
KUGE S (1); MORISHITA F (1); TSURUDA T (1); TOMISHIMA S (1); TSUKUDE M (1); YAMAGATA T (1); ARIMOTO K (1)
(1) Mitsubishi Electric Corp., Hyogo, JPN
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1996, VOL.E79-C,NO.7,
PAGE.997-1002, FIG.12, TBL.2, REF.12
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes a silicon on insulator (SOI) **DRAM** which has a body bias controlling technique for high-speed circuit operation and a new type of redundancy for low standby power operation, aimed at high yield. The body bias controlling technique contributes to super-body synchronous sensing and body-bias controlled logic. The super-body synchronous sensing achieves 3.0 ns faster sensing than body synchronous sensing and the body-bias controlled logic realizes 8.0 ns faster peripheral logic operation compared with a conventional logic scheme, at 1.5 V in a 4 Gb-level SOI **DRAM**. The body-bias

controlled logic also realizes a body-bias change current reduction of 1/20, compared with a bulk well-structure. A new type of redundancy that overcomes the standby current failure resulting from a **wordline-bitline** short is also discussed in respect of yield and area penalty. (author abst.)

13/3,AB/21 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02987936 JICST ACCESSION NUMBER: 96A0705411 FILE SEGMENT: JICST-E
Fault-Tolerant Designs for 256 Mb **DRAM**.
KIRIHATA T (1); WONG H (1); DEBROSSE J K (1); WORDEMAN M R (1); PARKE S A (1); WATANABE Y (2); YOSHIDA M (2); ASAO Y (2); POECHMUELLER P (3)
(1) IBM Semiconductor Res. and Dev. Center, NY, USA; (2) Toshiba, NY, USA ; (3) Siemens, NY, USA
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1996, VOL.E79-C,NO.7, PAGE.969-977, FIG.11, TBL.1, REF.27
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes fault-tolerant designs, which have been used to boost the yield of a 286 mm2 256 Mb **DRAM** with *32 both-ends DQ. The 256 Mb **DRAM** consists of sixteen 16 Mb units, each containing one 128 Kb row redundancy block. This row redundancy block architecture allows flexible row redundancy replacement, where random faults, clustered faults, and grouped faults can be efficiently repaired. Flexible column redundancy replacement with interchangeable master DQ's (MDQ) is used to allow a 256 b data compression without causing a data conflict, while improving the column access speed by 2 ns. A depletion **NMOS bitline**-precharge-current-limiter suppresses the current flow which occurs as a result of a **wordline-bitline** short-circuit to only 15 .MU.A per cross fail, avoiding a standby current fail. Consequently, the hardware results show a significant yield enhancement of 16 times relative to the intra-block/segment replacement. Detailed simulation results show that this 256 Mb **DRAM** allows 275 random faults to be repaired with 5.5% silicon area overhead for 80% chip yield. (author abst.)

13/3,AB/22 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02803136 JICST ACCESSION NUMBER: 96A0739517 FILE SEGMENT: JICST-E
Reversed-STacked-Capacitor(RSTC) **DRAM** Cell Suitable for **Embedded DRAM**'s.
SASAKI N (1); NAKAMURA S (1); HORIE H (1); NARA Y (1); ASANO K (1); FUKANO T (1)
(1) Fujitsu Lab. Ltd., Atsugi, JPN
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1996, VOL.96,NO.151(SDM96 50-56), PAGE.9-16, FIG.10, TBL.1, REF.5
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77

LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes a novel reversed-stacked-capacitor(RSTC) cell structure for Giga-bit **DRAM**'s. A storage capacitor and a **MOSFET** of a stacked-capacitor(STC) cell are reversed by using chemical-mechanical-polishing(CMP) and bonded-SOI technology. The **bit-lines** and metal wirings are realized on the flat surface with low-aspect-ratio contact holes throughout the whole chip. This cell structure is suitable for not only Giga-bit **DRAM**'s but also **embedded DRAM**'s. A test memory array is fabricated with a 64 Mbit **DRAM** design rule. Both capacitance and resistance of **bit-lines** are drastically decreased by a factor of two compared to the conventional shielded-**bit-line** STC cells. The **bit-lines** are placed far from **word-lines** and cell-capacitors. The **bit-lines** are made of low resistivity materials after all the high-temperature processes. (author abst.)

13/3,AB/23 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02760616 JICST ACCESSION NUMBER: 96A0462125 FILE SEGMENT: JICST-E
Semiconductor Devices. 1G bit **DRAM** for File Applications.
MUROTANI TATSUNORI (1); SUGIBAYASHI TADAHIKO (1); NARITAKE ISAO (1); UTSUGI SATOSHI (1); KOYAMA KUNIAKI (1)
(1) NEC ULSIDebaisukaiken
NEC Giho(NEC Technical Journal), 1996, VOL.49,NO.3, PAGE.12-15, FIG.6, TBL.1, REF.7
JOURNAL NUMBER: G0475BAB ISSN NO: 0285-4139
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: NEC has developed the world's first 1G bit **DRAM** for file applications. The circuit technologies implemented in this device are described herein. Three key circuit technologies for 1G bit **DRAMs** are a time-shared offset cancel sensing scheme, a defective **word-line** Hi-Z standby scheme and a flexible multimacro architecture. In addition to these technologies, the diagonal **bit-line** cell and 2-stage pipeline circuit technique have been adopted in the **DRAM** design. Through a combination of these technologies, a twofold improvement in yield, a 30% chip size reduction and a 400MHz data rate can be achieved. A 1G bit **DRAM** with these features has been fabricated using 0.25.MU.m CMOS process technology. The chip size is 936mm2. (author abst.)

13/3,AB/24 (Item 6 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02729680 JICST ACCESSION NUMBER: 96A0027785 FILE SEGMENT: JICST-E
'96 latest semiconductor process technology. The appearance of1GDRAM,now. 1GDRAM for file application.

MUROTANI TATSUNORI (1); SUGIBAYASHI NAOHIKO (1)
(1) NEC Corp.
Gekkan Semiconductor World(Semiconductor World), 1995, VOL.14,NO.11, PAGE.39-44, FIG.8, REF.5
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77 681.327
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: The new technology was developed, and the subject **DRAM** was produced experimentally.1) By development of the time division offset cancel system and adoption of the inclined **bit line** cell, the chip size was reduced to 30%.2) By development of defective **word line** high-impedance and flexible multi- macroscopic system, the high yield-rate was enabled.3) By adoption of 2-stage pipeline circuit technique and 32 bit input/output, 400MB/s data transfer rate was realized. The trial manufacture was carried out in 0.25 .MU.m CMOS process, and the chip size was 936mm2.The consumption current is 68mA at 2V, 100MHz.

13/3,AB/25 (Item 7 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02536568 JICST ACCESSION NUMBER: 95A0527542 FILE SEGMENT: JICST-E
Next generation device technology at ISSCC 95.1Gbit **DRAM most** suitable for a file memory.
MUROTANI TATSUNORI (1); SUGIBAYASHI TADAHIKO (1)
(1) NEC ULSIDebaisukaiken
Denshi Zairyo(Electronic Parts and Materials), 1995, VOL.34,NO.6, PAGE.27-31, FIG.9, REF.7
JOURNAL NUMBER: F0040AAH ISSN NO: 0387-0774
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: Three circuits techniques, such as offset cancel sense system, flexible multi- macroscopic system and bad **word line** high impedance system, suitable for the large-capacity **DRAM** are developed. One Gbit **DRAM**, using a skew **bit line** memory ell and a two-stage pipelined circuit, with a chip area 30% smaller than that of conventional system, achieving a yield of two tmes and suitable for a file memory, is developed. The chip size of 1Gbit **DRAM** produced experimentally using CMOS process of the 0.25.MU.m rules is 936mm2, and the data transfer rate at operating frequency 100MHz is 400MB/s.

13/3,AB/26 (Item 8 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01721012 JICST ACCESSION NUMBER: 93A0237858 FILE SEGMENT: JICST-E
A Buried Capacitor **DRAM** Cell with Bonded SOI.
IKEDA NAOSHI (1); NISHIHARA TOSHIYUKI (1); AOZASA HIROSHI (1); MIYAZAWA YOSHIHIRO (1); OCHIAI AKIHIKO (1)

(1) Sony Corp.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1993, VOL.92,NO.424(SDM92 137-149), PAGE.15-20, FIG.10, REF.7
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77 681.327
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: We proposed a novel **DRAM** cell structure using bonded SOI named a Buried Capacitor **DRAM** cell(BC cell). Since the cell capacitor is completely buried under the thin silicon layer, it is flexibly formed like stack-capacitor, resulting in a large cell capacitance. The BC cell needs no extra layout area except that for **bit-line** and **word-line** on the silicon surface.
Thus, the cell size is easily minimized to 8F2 for the folded **bit -line** structure. Moreover the cell leakage current is reduced to 1fA/cell using a SOI **PMOS** cell transistor whose back-surface is shielded by a cell plate. The BC cell can realize 256M bit **DRAM** and beyond. (author abst.)

13/3,AB/27 (Item 9 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01556285 JICST ACCESSION NUMBER: 92A0350881 FILE SEGMENT: JICST-E
A Pulsed Sensing Scheme with a Limited **Bit-Line** Swing.
SCHEUERLEIN R E (1); KATAYAMA Y (1); KIRIHATA T (1); SAKAUE Y (1); SATOH A (1); SUNAGA T (2); YOSHIKAWA T (2); KITAMURA K (2); DHONG S H (3)
(1) IBM Japan, Ltd., Tokyo, JPN; (2) IBM Japan, Yasu, JPN; (3) IBM Research, NY
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1992, VOL.E75-C,NO.4, PAGE.576-580, FIG.5, TBL.1, REF.8
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77 681.327
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication
ABSTRACT: This paper presents a pulsed sensing scheme with a limited **bit-line** swing designed for 4-Mb CMOS high-speed **DRAM** 's(HSDRAM's) and beyond. It uses a standard CMOS cross-coupled sense amplifier and limits the swing by means of a pulsed sense clock. The signal loss that would occur if the **bitline** swing was not exactly limited to one threshold above the **word-line**'s low level is avoided by using a small reference voltage negerator and trench decoupling capacitors. The new sensing scheme was successufully implemented on an experimental HSDRAM fabricated by using 0.7-.MU.m Leff CMOS technology, and thus a high-speed random access time of 15ns and a low power dissipation of 144mW were obtained for 512-kb array activation with a fast cycle time of 60ns at 3.6V. (author abst.)

23/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

01558362 INSPEC Abstract Number: B80039984
Title: A **silicon** and aluminum **dynamic memory** technology
Author(s): Larsen, R.A.
Author Affiliation: IBM General Technol. Div. Lab., Essex Junction, VT, USA
Journal: IBM Journal of Research and Development vol.24, no.3 p. 268-82
Publication Date: May 1980 Country of Publication: USA
CODEN: IBMJAE ISSN: 0018-8646
Language: English
Abstract: The **Silicon** and Aluminum **Metal Oxide Semiconductor** (SAMOS) technology is presented as a high-yield, low-cost process to make one-device-cell random access memories. The characteristics of the process are a multilayer dielectric **gate** insulator (oxide-nitride), a p-type **polysilicon** field shield, and a doped oxide diffusion source. Added yield-enhancing features are backside ion **implant** gettering, dual dielectric insulators between metal layers, and circuit redundancy. A family of chips is produced using SAMOS, **ranging** from 18K bits to 64K bits. System features such as on-chip data registers are designed on some chips. The chip technology is merged with 'flip-chip' packaging to provide one-inch-square modules from 72K bits through 512K bits, with typical access times from 90 ns to 300 ns.
Subfile: B

23/3,AB/2 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04464733
E.I. No: EIP96083273086
Title: Design and performance of SOI pass transistors for 1Gbit **DRAMs**
Author: Hu, Yin; Teng, Clarence W.; Houston, Ted W.; Joyner, Keith; Aton, Tom J.
Corporate Source: Texas Instruments Inc, Dallas, TX, USA
Conference Title: Proceedings of the 1996 Symposium on VLSI Technology
Conference Location: Honolulu, HI, USA Conference Date: 19960611-19960613
E.I. Conference No.: 45102
Source: Digest of Technical Papers - Symposium on VLSI Technology 1996. IEEE, Piscataway, NJ, USA,96CH35944. p 128-129
Publication Year: 1996
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: Both partially and fully depleted **NMOS** pass transistors were designed and fabricated on SIMOX substrates. Using a p plus **gate** design, V//t//h approximately equals 1V and I//o//f//f less than 1fA/ mu m was achieved on ultra thin film SOI pass transistors. With less than 1fA/ mu m off-state leakage, the SOI pass transistor provides excellent **DRAM** cell retention time and low stand-by power. The pass transistor's junction voltage decay after precharge is much slower on the thin film SOI than on thicker film SOI. In addition, the SOI pass transistors were found to have higher **DRAM** charging efficiency than

the bulk pass transistor due to the elimination of the **body** effect. The higher charging efficiency of SOI pass transistors allows a reduction in the word line voltage during the charging state, avoiding the need for the usual boosting of the **DRAM** word line voltage, thereby increasing the **gate** oxide integrity and decreasing the active power. (Author abstract) 2 Refs.

23/3,AB/3 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04945819 JICST ACCESSION NUMBER: 01A0700041 FILE SEGMENT: JICST-E
Dual-Thickness **Gate** Oxidation Technology with Halogen/Xenon **Implantation** for **Embedded Dynamic Random** Access **Memories**.
SUGIZAKI T (1); NAKANISHI T (1); MURAKOSHI A (2); OZAWA Y (2); SUGURO K (2)
(1) Fujitsu Lab., Ltd., Yokohama, Jpn; (2) Toshiba Corp., Yokohama, Jpn
Jpn J Appl Phys Part 1, 2001, VOL.40,NO.4B, PAGE.2674-2678, FIG.13, REF.6
JOURNAL NUMBER: G0520BAE ISSN NO: 0021-4922
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: We investigated the enhanced oxidation effect of using **silicon**(Si) **implanted** with fluorine(F), iodine(I), and xenon(Xe) before **gate** oxidation. I and Xe, which result in shallower **implants** because of their higher mass numbers, were expected to be less damaging to the Si substrate. The resultant increase in oxide thickness was found to be 20%, 80%, and 50% under F, I, and Xe **implantations** with a dose of 5*1014cm-2, respectively. We found that F atoms outdiffuse to their ambient through Si02, and that I **implantation** causes the greatest increase in oxide thickness. In addition, F **implantation** shows highly reliable dielectric characteristics, low contact resistance, and a low junction leakage current. Consequently, the F **implantation** process is capable of providing reliable dual-thickness **gate** oxide for **embedded dynamic random** access **memories**(**DRAMs**). (author abst.)

23/3,AB/4 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03941787 JICST ACCESSION NUMBER: 99A0007072 FILE SEGMENT: JICST-E
0.25.MU.m W-Polycide Dual **Gate** and Buried Metal on Diffusion Layer(BMD) Technology for **DRAM-Embedded** Logic Devices.
TSUKAMOTO M (1); KURODA H (1); OKAMOTO Y (1)
(1) Sony Corp.
Proc Sony Res Forum, 1998, VOL.7th, PAGE.381-385, FIG.12, REF.7
JOURNAL NUMBER: L1705AAQ ISSN NO: 1340-3508
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

23/3,AB/5 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01064638 JICST ACCESSION NUMBER: 90A0613878 FILE SEGMENT: JICST-E
Study on **implanted** ion channeling through **gate polysilicon** using **DRAM** cell.
KUMAGAI JUNPEI (1); SUGIURA SOICHI (1); SAWADA SHIZUO (1); SHINOZAKI SATOSHI (1)
(1) Toshiba Corp., Semiconductor Device Engineering Lab.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1990, VOL.90,NO.109(SDM90 36-48), PAGE.67-72, FIG.10, REF.3
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.08
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

27/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

5934350 INSPEC Abstract Number: B9807-1265D-030
Title: Source-bias dependent charge accumulation in p/sup +/-poly **gate** SOI **dynamic** **random** access **memory** cell transistors
Author(s): Jai-Hoon Sim; Kinam Kim
Author Affiliation: Semicond. R&D Centre, Samsung Electron. Co., Kyungki-Do, South Korea
Journal: Japanese Journal of Applied Physics, Part 1 (Regular Papers, Short Notes & Review Papers) Conference Title: Jpn. J. Appl. Phys. 1, Regul. Pap. Short Notes Rev. Pap. (Japan) vol.37, no.3B p.1260-3
Publisher: Publication Office, Japanese Journal Appl. Phys,
Publication Date: March 1998 Country of Publication: Japan
CODEN: JAPNDE ISSN: 0021-4922
SICI: 0021-4922(199803)37:3BL.1260:SBDC;1-E
Material Identity Number: F221-98006
Conference Title: Solid State Devices and Materials
Conference Date: 16-19 Sept. 1997 Conference Location: Hamamatsu, Japan
Language: English
Abstract: In this paper, we report the dynamic data retention problems caused by the transient leakage current in a cell transistor during the **bit-line** pull down operation in p/sup +/-poly **gate** fully depleted **silicon**-on-insulator (FD-SOI) **dynamic** **random** access **memories** (**DRAMs**) due to the source-induced charge accumulation (SICA) effect in the **silicon** thin film. Due to the inherent floating body effect in the FD-SOI transistor, charge accumulation in the **silicon** thin film becomes inevitable when the **gate** -to-source voltage (V/sub GS/) is smaller than the flat-band voltage (V/sub FB/). In order to eliminate the transient leakage current problem in p/sup +/-poly **gate** FD-SOI cell transistor, the ground-precharged **bit-line** (GPB) sensing method is introduced.
Subfile: B

27/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

02144665 INSPEC Abstract Number: B83059848
Title: A new **dynamic** **random** access **memory** cell using a bipolar **MOS** composite structure
Author(s): Wu, C.-Y.
Author Affiliation: Inst. of Electronics, Nat. Chiao Tung Univ., Hsin-Chu, Taiwan
Journal: IEEE Transactions on Electron Devices vol.ED-30, no.8 p. 886-94
Publication Date: Aug. 1983 Country of Publication: USA
CODEN: IETDAI ISSN: 0018-9383
U.S. Copyright Clearance Center Code: 0018-9383/83/0800-0886$01.00
Language: English
Abstract: A new **dynamic** **RAM** cell which incorporates an n-p-n bipolar junction transistor with an n-channel **MOSFET** in a composite structure, is proposed and investigated. In this novel cell called the

BIMOS cell, the collector-base junction serves as a buried storage capacitor and the n-**MOSFET** as a transfer **gate**. The fabrication technology is simple and compatible with that of single-**polysilicon** CMOS ICs and a minimum cell size of 14.875 F/sup 2/ where F is minimum feature size realizable. The write, read, and standby operations of the cell are analyzed and simulated. An experimental cell is fabricated and characterized. It is shown that large storage capacitance to **bit-line** capacitance ratio as well as fairly good packing density, soft-error immunity and leakage characteristics are expected. Compared to the conventional 1-transistor cell the new cell can be scaled down with less processing trouble and better performance. Simple process and good scaled-down properties offer great potential for VLSI RAM.

Subfile: B

27/3,AB/3 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS

1777204 NTIS Accession Number: N94-15640/3

Fault Handling Schemes in Electronic Systems with Specific Application to Radiation Tolerance and VLSI Design

(Final Report, 3 Jan. 1989 - Oct. 1993)

Attia, J. O.

Prairie Observatory, Urbana, IL. College of Engineering and Architecture.

Corp. Source Codes: 888888888; P0782089

Sponsor: National Aeronautics and Space Administration, Washington, DC.

Report No.: NAS 1.26:194559; NASA-CR-194559

Oct 93 106p

Languages: English

Journal Announcement: GRAI9405; STAR3203

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Naturally occurring space radiation particles can produce transient and permanent changes in the electrical properties of electronic devices and systems. In this work, the transient radiation effects on **DRAM** and CMOS SRAM were considered. In addition, the effect of total ionizing dose radiation of the switching times of CMOS logic **gates** were investigated. Effects of transient radiation on the column and cell of **MOS dynamic memory** cell was simulated using SPICE. It was found that the critical charge of the **bitline** was higher than that of the cell. In addition, the critical charge of the combined cell-**bitline** was found to be dependent on the **gate** voltage of the access transistor. In addition, the effect of total ionizing dose radiation on the switching times of CMOS logic **gate** was obtained. The results of this work indicate that, the rise time of CMOS logic **gates** increases, while the fall time decreases with an increase in total ionizing dose radiation. Also, by increasing the size of the P-channel transistor with respect to that of the N-channel transistor, the propagation delay of CMOS logic **gate** can be made to decrease with, or be independent of an increase in total ionizing dose radiation. Furthermore, a method was developed for replacing **polysilicon** feedback resistance of SRAMs with a switched capacitor network. A switched capacitor SRAM was implemented using **MOS** Technology. The critical change of the switched capacitor SRAM has a very large critical charge. The results of this work indicate that switched capacitor SRAM is a viable alternative to SRAM with

polysilicon feedback resistance.

27/3,AB/4 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05533175
E.I. No: EIP00045134686
Title: Mechanisms of dynamic pass leakage current in partially depleted SOI **MOSFETs**
Author: Saraya, T.; Hiramoto, T.
Corporate Source: Univ of Tokyo, Tokyo, Jpn
Conference Title: The 25th Annual IEEE International Silicon-on-Insualtor (SOI) Conference
Conference Location: Rohnert Park, CA, USA Conference Date: 19991004-19991007
E.I. Conference No.: 56659
Source: IEEE International SOI Conference 1999. IEEE, Piscataway, NJ, USA. p 84-85
Publication Year: 1999
CODEN: IISPED
Language: English
Abstract: The dynamic pass leakage current in partially depleted (PD) **silicon** on insulator (SOI) **MOSFETs** has been investigated. Contributions of bipolar and subthreshold current are successfully separated by transient measurements of the **gate** bias dependence. It is found that the subthreshold current is dominant in the dynamic pass leakage in typical **dynamic random** access **memory** (**DRAM**) conditions. The bipolar current arises only when the pulse period is longer than 0.1 s. Reducing the coupling between **word lines** rather than reducing bipolar gain is effective for the suppression of the dynamic pass leakage. 7 Refs.

27/3,AB/5 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

06736103 Genuine Article#: ZN627 Number of References: 10
Title: Source-bias dependent charge accumulation in P+-poly **gate** SOI **dynamic random** access **memory** cell transistors (ABSTRACT AVAILABLE)
Author(s): Sim JH (REPRINT) ; Kim K
Corporate Source: SAMSUNG ELECT CO,SEMICOND R&D CTR/YONGIN/KYUNGKI DO/SOUTH KOREA/ (REPRINT)
Journal: JAPANESE JOURNAL OF APPLIED PHYSICS PART 1-REGULAR PAPERS SHORT NOTES & REVIEW PAPERS, 1998, V37, N3B (MAR), P1260-1263
ISSN: 0021-4922 Publication date: 19980300
Publisher: JAPAN J APPLIED PHYSICS, DAINI TOYOKAIJI BLDG 24-8 SHINBASHI 4-CHOME, MINATO-KU TOKYO 105, JAPAN
Language: English Document Type: ARTICLE
Abstract: In this paper, we report the dynamic data retention problems caused by the transient leakage current in a cell transistor during the **bit-line** pull down operation in pi-poly **gate** fully depleted **silicon**-on-insulator (FD-SOT) **dynamic random** access **memories** (**DRAMs**) due to the source-induced charge accumulation (SICA) effect in the **silicon** thin film. Due to the inherent floating body effect in the FD-SOI transistor, charge

accumulation in the **silicon** thin film becomes inevitable when the **gate**-to-source voltage (V-GS) is Smaller than the hat-band voltage (V-FB). In order to eliminate the transient leakage current problem in p(+)-poly **gate** FD-SOI cell transistor, the ground-precharged **bit-line** (GPB) sensing method is introduced.

27/3,AB/6 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01812306 AADAAI3001985
Recrystallized **silicon** pillar **MOSFETs** for high density **DRAM** cells
Author: Cho, Hyun Jin
Degree: Ph.D.
Year: 2001
Corporate Source/Institution: Stanford University (0212)
Source: VOLUME 62/01-B OF DISSERTATION ABSTRACTS INTERNATIONAL. PAGE 414. 182 PAGES
ISBN: 0-493-10846-7

Dynamic random access **memory** (**DRAM**) is an important technology driver for the semiconductor industry. In order to meet industry demands to store larger and larger amounts of data in a small chip area, devices have had to be continuously scaled down. For **DRAM** devices beyond 4 Gigabits however, the conventional method of fabrication will no longer be viable because of the high subthreshold leakage current in the access transistors. The objective of this thesis work is to investigate potential solutions to this problem by developing a new recrystallized **silicon** pillar transistor.

A recrystallized-Si pillar (vertical) transistor is formed on top of a trench capacitor with the top of the pillar transistor directly connected to the **bit line**. This vertical structure forms a 4F<super>2</super> cell reducing the cell area of a conventional 8F<super>2</super> cell by half. The proposed fabrication processes are far simpler and require fewer mask steps than conventional **DRAM** cell technology.

The material properties of recrystallized-Si pillars were investigated by cross sectional TEM analysis. As the pillar size decreased, the probability of obtaining a single grain structure increased. The mechanisms behind single grain formation were heterogeneous nucleation at the bottom of the pillar and an orientation dependent growth rate.

An analytical model for surrounding **gate MOSFETs** including bulk traps was investigated. Based on the depletion approximation and the assumption that bulk traps are uniformly distributed inside the bandgap, Poisson's equation in cylindrical coordinates was solved. The model predicts that the threshold voltage and subthreshold swing increase as the trap density increases. The analytical solution yields good agreement with MEDICI simulations confirming the model.

Electrical measurements showed that the recrystallized-Si pillar transistor exhibits good subthreshold slope and Id-Vd characteristics. Improvements in the device performance were achieved by sacrificial oxidation and hydrogenation. By controlling the channel doping and **gate** oxide thickness, partially depleted (PD) and fully depleted (FD) transistors were fabricated.

Materials analysis, modeling, and measured device characteristics indicated that device performance improves with scaling. Therefore,

recrystallized-Si pillar **MOSFETs** are a promising candidate for future **DRAM** access transistors.

27/3,AB/7 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05177521 JICST ACCESSION NUMBER: 02A0597345 FILE SEGMENT: PreJICST-E
Analysis of Analog Capacitor for Mixed Signal Circuits in Merged **Dynamic Random** Access **Memory** and Logic Devices.
JANG M G (1); LEE J H (2)
(1) Electronics And Telecommunications Res. Inst., Daejon, Kor; (2) Hynix Semiconductor Inc., Chungcheong-buk-do, Kor
Jpn J Appl Phys Part 2, 2002, VOL.41,NO.6B, PAGE.L675-L677
JOURNAL NUMBER: F0599BAD ISSN NO: 0021-4922
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
MEDIA TYPE: Printed Publication
ABSTRACT: A poly-insulator-poly(PIP) analog capacitor with a novel structure is fabricated to minimize the number of process steps by adopting an analog device in the merged **dynamic random** access **memory(DRAM)** and logic (MDL) process. It has **polysilicon** as the bottom electrode, which is used as the **gate** material of the transistor, and W-polycide as the top electrode, which is used as a **bit line** material in **DRAM**. The area capacitance without the fringe effect is 0.54fF/.MU.m2 and the leakage current is less than 1fA/.MU.m2. The minimum usable capacitor size without the fringe effect is 27*27.MU.m2. The voltage coefficients of the 1st and 2nd order are 380ppm/V and -11ppm/V2, respectively, where those of a conventional analog capacitor manufactured by the standard complementary **metal oxide semiconductor**(CMOS) process are 300-500ppm/V and 10-50ppm/V2, respectively. The matching value is 0.044% in an area of 27*27.MU.m2, which is an excellent result compared with previous work. (author abst.)

27/3,AB/8 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02317400 JICST ACCESSION NUMBER: 95A0394230 FILE SEGMENT: JICST-E
Special Issue on Semiconductor Devices. Process and Device Technologies for 1G bit **DRAM** Cells.
OIKAWA RYUICHI (1); NAKAJIMA KEN (1); MORI HIDEMITSU (1); KOYAMA KUNIAKI (1); SHIBAHARA KENTARO (2)
(1) NEC ULSIDebaisukaiken; (2) Hiroshima Univ.
NEC Giho(NEC Technical Journal), 1995, VOL.48,NO.3, PAGE.188-192, FIG.10, TBL.1, REF.4
JOURNAL NUMBER: G0475BAB ISSN NO: 0285-4139
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: New stacked capacitor cells for 1Gb **DRAMs** have been fabricated. Diagonal-**bit-line**(DBL) configuration has reduced cell area down to 75% compared with conventional cells. An edge

operation **MOS**(EOS) FET has been developed for cell transfer **gates** which is suitable for low-voltage operation. The 0.375.MU.m2 cells were fabricated with 0.2.MU.m fabrication technologies. A storage capacitance of 28.5fF was obtained with a Ta2O5 dielectric film on hemi-spherical grained **silicon** (HSG-Si) cylinders. (author abst.)

29/3,AB/1 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04412486 JICST ACCESSION NUMBER: 00A0066770 FILE SEGMENT: JICST-E
IEDM 99.
KAWANE TOSHIAKI (1)
Gekkan Semiconductor World(Semiconductor World), 1999, VOL.18,NO.12, PAGE.74-75, FIG.2
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: IEDM'99 (Washington D.C. on 12/5-12/9th, 1999)was held. This is a report from the meeting. This time, there was a proposal of the epoch-making transistor structure in CMOS device in which the limit for the refinement began to be seen from the viewpoint of power consumption and lithography. It is a transistor (VRG **MOSFET**) of the vertical structure in which gate,source and drain are fabricated **perpendicularly** to the substrate. Lucent Technology reported a transistor of the 50nm gate length and Infineon/IBM reported a vertical transistor (VERI VEST) for the **DRAM** trench cell.

33/3,AB/1 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC

7239067 INSPEC Abstract Number: B2002-05-2560R-081
Title: SON (**Silicon** on Nothing) **MOSFET** using ESS (Empty Space in **Silicon**) technique for SoC applications
Author(s): Sato, T.; Nii, H.; Hatano, M.; Takenaka, K.; Hayashi, H.; Ishigo, K.; Hirano, T.; Ida, K.; Aoki, N.; Ohguto, T.; Ino, K.; Mizushima, I.; Tsunashima, T.
Author Affiliation: Process & Manuf. Eng. Center, Toshiba Corp., Yokohama, Japan
Conference Title: International Electron Devices Meeting. Technical Digest (Cat. No.01CH37224) p.37.1.1-4
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA 951 pp.
ISBN: 0 7803 7050 3 Material Identity Number: XX-2002-00101
U.S. Copyright Clearance Center Code: 0-7803-7050-3/01/$10.00
Conference Title: International Electron Devices Meeting. Technical Digest
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 2-5 Dec. 2001 Conference Location: Washington, DC, USA
Language: English
Abstract: SON (**Silicon** on Nothing) **MOSFET** was successfully fabricated for the first time by using ESS (Empty Space in **Silicon**) technique as an alternative of SOI-**MOSFET**. Advantage of SON structure was experimentally demonstrated. SON structure using ESS technique is appropriate for System on a Chip (SoC) applications, such as **embedded** trench **DRAMs** and digital-analog mixed devices, due to the merit that SON structure can be fabricated partially on bulk substrate.
Subfile: B
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33/3,AB/2 (Item 2 from file: 2)
DIALOG(R)File 2:INSPEC

7176140 INSPEC Abstract Number: B2002-03-1265D-023
Title: 0.15 mu m SOI **DRAM** technology incorporating sub-volt dynamic threshold devices for **embedded** mixed-signal & RF circuits
Author(s): Goldman, D.; DeGregorio, K.; Kim, C.S.; Nielson, M.; Zahurak, J.; Parke, S.
Author Affiliation: Dept. of Electr. & Comput. Eng., Boise State Univ., ID, USA
Conference Title: 2001 IEEE International SOI Conference. Proceedings (Cat. No.01CH37207) p.97-8
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2001 Country of Publication: USA x+158 pp.
ISBN: 0 7803 6739 1 Material Identity Number: XX-2001-02297
U.S. Copyright Clearance Center Code: 0-7803-6739-1/01/$10.00
Conference Title: 2001 IEEE International SOI Conference. Proceedings
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 1-4 Oct. 2001 Conference Location: Durango, CO, USA
Language: English
Abstract: This paper describes the DC and high frequency characteristics of a low-cost, 0.15 mu m PDSOI **DRAM** technology. A compact dynamic

threshold (DT) device design in this process is found to be superior to both grounded body (GB) and floating body (FB) PD-SOI **MOSFETs**. This device achieves kink-free behavior, with gm=936 mu S/um, g/sub out/=36 mu S/um, Ion/Ioff=210 mu A/0.1 pA, S=67 mV/dec, and fmax=32 GHz at V/sub DD/=1 V. These DTMOS devices are excellent for sub-volt **embedded** baseband and IF circuits and sufficient for RF front-end circuits, thus enabling the combination of **embedded DRAM**, digital, analog and RF circuit cores in, ultra-low-power, low-cost SOCs.
Subfile: B

33/3,AB/3 (Item 3 from file: 2)
DIALOG(R)File 2:INSPEC

7171575 INSPEC Abstract Number: B2002-03-1265D-015, C2002-03-5320G-009
Title: A capacitor-less 1T-**DRAM** cell
Author(s): Okhonin, S.; Nagoga, M.; Sallese, J.M.; Fazan, P.
Author Affiliation: Signal Process. Lab., LEG, Lausanne, Switzerland
Journal: IEEE Electron Device Letters vol.23, no.2 p.85-7
Publisher: IEEE,
Publication Date: Feb. 2002 Country of Publication: USA
CODEN: EDLEDZ ISSN: 0741-3106
SICI: 0741-3106(200202)23:2L.85:CLDC;1-G
Material Identity Number: I338-2002-003
U.S. Copyright Clearance Center Code: 0741-3106/02/$17.00
Language: English
Abstract: A simple true 1 transistor **dynamic random** access **memory** (**DRAM**) cell concept is proposed for the first time, using the body charging of partially-depleted SOI devices to store the logic "1" or "0" binary states. This cell is two times smaller in area than the conventional 8F/sup 2/ 1T/1C **DRAM** cell and the process of its manufacturing does not require the storage capacitor fabrication steps. This concept will allow the manufacture of simple low cost **DRAM** and **embedded DRAM** chips for 100 and sub-100 nm generations.
Subfile: B C

33/3,AB/4 (Item 4 from file: 2)
DIALOG(R)File 2:INSPEC

6880863 INSPEC Abstract Number: B2001-05-1265D-020
Title: A novel bit-line process using poly-Si masked dual-damascene (PMDD) for 0.13 mu m **DRAMs** and beyond
Author(s): Miyashita, T.; Nitta, H.; Nomura, H.; Nakajima, K.; Sakata, A.; Mizutani, T.; Minakata, H.; Tanaka, M.; Tomita, H.; Kurahashi, T.; Watanabe, Y.; Kubota, T.; Hatada, A.; Hosaka, K.; Hashimoto, K.; Kohyama, Y.
Author Affiliation: Fujitsu Labs. Ltd., Yokohama, Japan
Conference Title: International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138) p.361-4
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 2000 Country of Publication: USA 871 pp.
ISBN: 0 7803 6438 4 Material Identity Number: XX-2001-00191
U.S. Copyright Clearance Center Code: 0 7803 6438 4/2000/$10.00
Conference Title: International Electron Devices Meeting. Technical

Digest. IEDM
Conference Sponsor: Electron Devices Soc. IEEE
Conference Date: 10-13 Dec. 2000 Conference Location: San Francisco, CA, USA
Language: English
Abstract: A novel middle-of-line (MOL) **DRAM** cell technology based on the poly-Si masked dual-damascene tungsten bit-line (BL) has been developed. New technologies such as borderless rectangular metal contacts, a thermally robust tri-layer barrier metal, well-controlled dry/wet recessed damascene BLs, and a low-temperature LPCVD-Si/sub 3/N/sub 4/ cap for a storage node self-aligned contact make it possible to realize the successful MOL integration for 0.13 mu m **DRAMs**. Since this process offers a sufficient alignment margin and a significant reduction of chip size as well as a reduced thermal budget, it is expected to be useful for making the future gigabit **DRAMs** and logic **embedded DRAMs**.

Subfile: B

33/3,AB/5 (Item 5 from file: 2)
DIALOG(R)File 2:INSPEC

6189822 INSPEC Abstract Number: B1999-04-1265D-056
Title: Integration of trench **DRAM** into a high-performance 0.18 mu m logic technology with copper BEOL
Author(s): Crowder, S.; Hannon, R.; Ho, H.; Sinitsky, D.; Wu, S.; Winstel, K.; Khan, B.; Stiffler, S.R.; Iyer, S.S.
Author Affiliation: Microelectron. Div., IBM Corp., Hopewell Junction, NY, USA
Conference Title: International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217) p.1017-20
Publisher: IEEE, Piscataway, NJ, USA
Publication Date: 1998 Country of Publication: USA 1080 pp.
ISBN: 0 7803 4774 9 Material Identity Number: XX-1999-00230
U.S. Copyright Clearance Center Code: 0 7803 4774 9/98/$10.00
Conference Title: International Electron Devices Meeting 1998. Technical Digest
Conference Sponsor: IEEE Electron Devices Soc
Conference Date: 6-9 Dec. 1998 Conference Location: San Francisco, CA, USA
Language: English
Abstract: In this work, we demonstrate the integration of trench **DRAM** into a 0.18 mu m copper BEOL technology which is fully compatible with our **most** advanced logic technology and requires no redesign of preexisting logic circuitry. This technology offers a 0.617 mu m/sup 2/ **DRAM** cell on the same chip as a 4.2 mu m/sup 2/ SRAM cell and dual damascene copper metallization with the highest reported device performance for a 1.5 V bulk **silicon** technology. We demonstrate a fixable retention time of over 256 ms at 85 degrees C for the **DRAM** cell without any degradation in logic device performance or density.
Subfile: B

33/3,AB/6 (Item 6 from file: 2)
DIALOG(R)File 2:INSPEC

5687136 INSPEC Abstract Number: B9710-2550B-039
Title: Evaluation of micro-defects by **DRAM** data retention characteristics measurement
Author(s): Miyoshi, K.; Terashima, K.; Muramatsu, Y.; Nishio, N.; Murotani, T.; Saito, S.
Author Affiliation: ULSI Device Dev. Lab., NEC Corp., Sagamihara, Japan
Journal: Nuclear Instruments & Methods in Physics Research, Section B (Beam Interactions with Materials and Atoms) Conference Title: Nucl. Instrum. Methods Phys. Res. B, Beam Interact. Mater. At. (Netherlands) vol.127-128 p.78-81
Publisher: Elsevier,
Publication Date: May 1997 Country of Publication: Netherlands
CODEN: NIMBEU ISSN: 0168-583X
SICI: 0168-583X(199705)127/128L.78:EMDD;1-S
Material Identity Number: G701-97015
U.S. Copyright Clearance Center Code: 0168-583X/97/$17.00
Conference Title: Ion Beam Modification of Materials. Tenth International Conference on Ion Beam Modification of Materials
Conference Sponsor: Elsevier; High Voltage Eng. Eur.; SEMATECH; Appl. Mater.; et al
Conference Date: 1-6 Sept. 1996 Conference Location: Albuquerque, NM, USA
Language: English
Abstract: The influence of micro-defects induced intentionally by Si/sup +/ ion **implantation** was investigated using data retention characteristics of **dynamic random** access **memory** (**DRAM**). The defect formation was controlled by Si/sup +/ **implantation** and subsequent annealing conditions. Micro-defects such as {311} defects having a size below 50 nm degraded the junction leakage current and data retention characteristics. Data retention characteristics was also affected by the existence of micro-defects such as point defect or its clusters, although the junction leakage current was low enough compared with unimplanted samples.
Subfile: B

33/3,AB/7 (Item 7 from file: 2)
DIALOG(R)File 2:INSPEC

02843658 INSPEC Abstract Number: B87017098
Title: Holding time distribution; an instrument for characterizing **MOS DRAMs**
Author(s): Lechner, P.; Kirchstetter, J.; Mohr, W.; Papp, A.
Author Affiliation: Siemens AG, Munich, West Germany
Conference Title: Proceedings of the Fifth International Symposium on Silicon Materials Science and Technology: Semiconductor Silicon 1986 p. 1065-73
Editor(s): Huff, H.R.; Abe, T.; Kolbesen, B.
Publisher: Electrochem. Soc, Pennington, NJ, USA
Publication Date: 1986 Country of Publication: USA xiv+1096 pp.
Conference Sponsor: Electrochem. Soc
Conference Date: 5-9 May 1986 Conference Location: Boston, MA, USA
Language: English
Abstract: A new method of characterizing **dynamic memories** was developed on the basis of the refresh test. It allows rapid determination of the failure mechanism of single cells or entire cell arrays. Comparative

investigations have shown that with clean process runs, memories on FZ **silicon** permit significantly longer refresh pauses than those on CZ **silicon**. This maximum holding time also depends greatly on the oxygen content of the substrate and can for instance also be influence by preannealing of CZ **silicon** or by performing a 'HiC' **implantation**.
Subfile: B

33/3,AB/8 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05967355
E.I. No: EIP01536782938
Title: 0.15um SOI **DRAM** technology incorporating sub-volt dynamic threshold devices for **embedded** mixed-signal & RF circuits
Author: Goldman, D.; DeGregorio, K.; Kim, C.S.; Nielson, M.; Zahurak, J.; Parke, S.
Corporate Source: Boise State University Dept. of Electrical and Comp. Eng., Boise, ID, United States
Conference Title: 2001 IEEE International SOI Conference
Conference Location: Durango, CO, United States Conference Date: 20011001-20011004
E.I. Conference No.: 58879
Source: IEEE International SOI Conference 2001. p 97-98 (IEEE cat n 01CH37207)
Publication Year: 2001
CODEN: IISPED
Language: English
Abstract: This paper describes the DC and high frequency characteristics of a low-cost, 0.15um PDSOI **DRAM** technology. A compact dynamic threshold (DT) device design in this process is found to be superior to both grounded body (GB) and floating body (FB) PDSOI **MOSFETs**. This device achieves kink-free behavior, with gm=936muS/um, g//o//u//t=36muS/um, Ion/Ioff=210muA/0.1pA, S=67mV/dec, and fmax=32GHz at V//D//D=1V. These DTMOS devices are excellent for sub-volt **embedded** baseband and IF circuits and sufficient for RF front-end circuits, thus enabling the combination of **embedded DRAM**, digital, analog, and RF circuit cores in, ultra-low-power, low-cost SOCs. 7 Refs.

33/3,AB/9 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05918112
E.I. No: EIP01436699586
Title: 2001 International symposium on VLSI technology, systems and applications
Author: Anon (Ed.)
Conference Title: 2001 International Symposium on VLSI Technology, Systems, and Applications, Proceedings
Conference Location: Hsinchu, Taiwan Conference Date: 20010418-20010420
E.I. Conference No.: 58553
Source: International Symposium on VLSI Technology, Systems, and Applications, Proceedings 2001. 311p (IEEE cat n 01TH8517)
Publication Year: 2001
Language: English

Abstract: The proceedings contains 80 papers from the 2001 International Symposium on VLSI Technology, Systems and Applications. The topics discussed include: System on a chip(SOC); **silicon** on insulator technology (SOI); nanoscale complementary **metal oxide semiconductor** (CMOS) circuits; low temperature capacitor technology for **embedded** dynamic random access storage (**DRAM**); low power finite impulse response (FIR) filter design technique for dynamic reduced signal representation and using Syndrome Compression for memory built-in Self-diagnosis. (Edited abstract)

33/3,AB/10 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05606121
E.I. No: EIP00075244116
Title: Characteristics of dual polymetal (W/WNx/Poly-Si) gate complementary **metal oxide semiconductor** for 0.1 mu m **dynamic random** access **memory** technology
Author: Kim, Yong-Hae; Chang, Sung-Keun; Kim, Seon-Soon; Choi, Jun-Gi; Lee, Sang-Hee; Hahn, Dae-Hee; Kim, Hyung-Duck
Corporate Source: Hyundai Electronics Industries, Kyungki-do, S Korea
Source: Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers v 39 n 5 B 2000. p 1969-1973
Publication Year: 2000
CODEN: JAPNDE ISSN: 0021-4922
Language: English
Abstract: We developed a dual polymetal (W/WNx/poly-Si) gate complementary **metal oxide semiconductor** (**MOS**) down to a 0.15 mu m gate length. The short-channel effects are effectively suppressed and a saturation current of 300 mu A/ mu m is obtained for **nMOS** and 110 mu A/ mu m is observed for **pMOS** at a 0.15 mu m gate length. The lower saturation current of **pMOS** is attributed both the p** plus -doped poly gate depletion and to the hole mobility degradation due to the increased vertical electric field in the surface-channel **pMOS**. Boron penetration is not observed with pure SiO//2 gate dielectrics. The gate induced drain leakage current could be markedly reduced by optimizing the well doping below the gate edge. (Author abstract) 14 Refs.

33/3,AB/11 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05516984
E.I. No: EIP00045106648
Title: Design and characterization of an **embedded** ASIC **DRAM**
Author: Birk, Gershom; Elliott, Duncan G.; Cockburn, Bruce F.
Corporate Source: Univ of Alberta, Edmonton, Alberta, Can
Conference Title: 1999 IEEE Canadian Conference on Electrical and Computer Engineering 'Engineering Solutions for the Next Millennium'
Conference Location: Edmonton, Alberta, Can Conference Date: 19990509-19990512
E.I. Conference No.: 56427
Source: Canadian Conference on Electrical and Computer Engineering v 1 1999. p 427-432
Publication Year: 1999

CODEN: CCCEFV ISSN: 0840-7789
Language: English
Abstract: University **DRAM** research is hindered by the lack of access to specialized commodity **DRAM** or blended logic-**DRAM** processes. In this paper we describe the design of an **embedded DRAM** in the 0.35 mu m TSMC logic process, available through the Canadian Microelectronics Corporation (CMC). Our test chip design used a variation of the HDRAM macro cells developed by MOSAID Technologies Inc. This paper describes the **DRAM** and gives some preliminary test results. (Author abstract) 4 Refs.

33/3,AB/12 (Item 5 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05412805
E.I. No: EIP99114893636
Title: Fully integrated **embedded DRAM** technologies with high performance logic and commodity **DRAM** cells for system-on-a-chip
Author: Koike, H.; Takato, H.; Hiyama, K.; Yoshida, S.; Harakawa, H.; Kokubun, K.; Shimabukuro, T.; Kato, S.; Tamaoki, M.; Okano, H.; Sato, H.; Morimasa, Y.; Yamamoto, T.; Tanaka, M.; Kumagai, J.; et al
Corporate Source: Toshiba Corp, Yokohama, Jpn
Conference Title: Proceedings of the 1999 International Symposium on VLSI Technology, Systems, and Applications
Conference Location: Taipei, Taiwan Conference Date: 19990607-19990610
E.I. Conference No.: 55504
Source: International Symposium on VLSI Technology, Systems, and Applications, Proceedings 1999. p 243-246
Publication Year: 1999
ISSN: 1524-766X
Language: English
Abstract: This paper demonstrates a process integration for high performance and small footprint **embedded DRAMs**. A trench capacitor cell and a self-aligned bit line contact are selected to maintain exactly the same size as commodity **DRAM** cells. The cell array region is covered with thin SiN barrier against salicidation. Ti-salicide source/drain is used in the Logic region. No retention time degradation and good circuit performance are confirmed. (Author abstract) 3 Refs.

33/3,AB/13 (Item 6 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05342887
E.I. No: EIP99084761231
Title: Proposal of a logic compatible merged-type gain cell for high-density **embedded DRAM**'s
Author: Mukai, Mikio; Hayashi, Yutaka; Komatsu, Yasutoshi
Corporate Source: Sony Corp, Kanagawa-ken, Jpn
Source: IEEE Transactions on Electron Devices v 46 n 6 1999. p 1201-1206
Publication Year: 1999
CODEN: IETDAI ISSN: 0018-9383
Language: English
Abstract: A new structure is proposed for a logic compatible merged-type **DRAM** gain cell, and device and process simulations are performed to verify the cell operation. This cell enables the realization of the memory

cell without direct use of capacitor, and is almost compatible with a conventional CMOS logic process. Therefore, it does not require new materials nor new processing equipment, and can be realized in less than 5% increase in process steps in comparison to the 50%-60% increase or more for logic **embedded DRAM**'s with a one-capacitor plus one-transistor cell. It can drastically improve '1' and '0' states' separation due to JFET ON/OFF effect of an n-channel region between two p** plus -gate regions. For the investigation of the proposed gain cell, detailed simulation is performed utilizing the simulation system well tuned to the actual 0.25- mu m logic process technology. Furthermore three transistors are merged into approximately one transistor area minimizing the cell size to almost one transistor area. Nondestructive read-out (NDRO) is possible resulting in smaller read cycle time since it does not need re-writing after reading-out. Smaller access time is also possible due to current sensing instead of charge sensing. (Author abstract) 5 Refs.

33/3,AB/14 (Item 7 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05252273
E.I. No: EIP99034599339
Title: Multiple-thickness gate oxide and dual-gate technologies for high-performance logic-**embedded DRAMs**
Author: Togo, M.; Noda, K.; Tanigawa, T.
Corporate Source: NEC Corp, Kanagawa, Jpn
Conference Title: Proceedings of the 1998 IEEE International Electron Devices Meeting
Conference Location: San Francisco, CA, USA Conference Date: 19981206-19981209
E.I. Conference No.: 49917
Source: Technical Digest - International Electron Devices Meeting 1998. IEEE, Piscataway, NJ, USA,98CH36217. p 347-348
Publication Year: 1998
CODEN: TDIMD5 ISSN: 0163-1918
Language: English
Abstract: We demonstrate new fabrication technologies for dual-gate CMOSFETs with multiple-thickness gate oxide. The process consists of two major parts: forming a multiple-thickness gate oxide by using Ar** plus and N** plus **implantation**, and impurity doping into dual-gate poly-Si by using self-aligned thermal oxidation. During the doping process, nitrogen distribution recoiling from a Si//3N//4 cap on a PMOSFET gate suppresses boron penetration. (Author abstract) 6 Refs.

33/3,AB/15 (Item 8 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04970697
E.I. No: EIP98034104365
Title: Proceedings of the 1997 International Electron Devices Meeting
Author: Anon (Ed.)
Conference Title: Proceedings of the 1997 International Electron Devices Meeting
Conference Location: Washington, DC, USA Conference Date: 19971207-19971210
E.I. Conference No.: 48095

Source: Proceedings of the IEEE Hong Kong Electron Devices Meeting 1997. IEEE, Piscataway, NJ, USA,97CH36103. 944p
Publication Year: 1997
CODEN: 002525
Language: English
Abstract: The proceedings contains 216 papers from the 1997 IEEE International Electron Devices Meeting. Topics discussed include: **embedded dynamic random** access **memory** technology; complementary **metal oxide semiconductor** devices; device interconnect technology; quantum electronics; single electron devices; detectors; sensors; display devices; flash memory technology; lasers; light emitting diodes; **silicon** on insulator technology; thin film transistor technology; and microelectromechanical devices.

33/3,AB/16 (Item 9 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04863051
E.I. No: EIP97113907073
Title: Suppression of bit-line-induced disturbance in SOI **DRAM**/SRAM cells by bipolar **embedded** source structure (BESS)
Author: Horiuchi, Masatada; Sakata, Takeshi; Kimura, Shin'ichiro
Corporate Source: Hitachi Ltd, Tokyo, Jpn
Conference Title: Proceedings of the 1997 Symposium on VLSI Technology
Conference Location: Kyoto, Jpn Conference Date: 19970610-19970612
E.I. Conference No.: 47245
Source: Digest of Technical Papers - Symposium on VLSI Technology 1997. IEEE, Piscataway, NJ, USA,97CH36114. p 157-158
Publication Year: 1997
CODEN: DTPTEW ISSN: 0743-1562
Language: English
Abstract: The disturbance of stored charges in SOI memory cells, which is caused by floating body effects, is fully suppressed by using an access transistor with a bipolar **embedded** source structure just beneath the n** plus junction. This structure is free from the subthreshold leakage current and degradation caused by high source resistance. (Author abstract)

33/3,AB/17 (Item 10 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04734474
E.I. No: EIP97073706143
Title: Proceedings of the 1996 MRS Fall Meeting
Author: Warren, W.L. (Ed.); Devine, R.A.B. (Ed.); Matsumura, M. (Ed.); Cristoloveanu, S. (Ed.); Homma, Y. (Ed.); Kanicki, J. (Ed.)
Corporate Source: Sandia National Laboratories, Albuquerque, NM, USA
Conference Title: Proceedings of the 1996 MRS Fall Meeting
Conference Location: Boston, MA, USA Conference Date: 19961202-19961204
E.I. Conference No.: 46250
Source: Amorphous and Crystalline Insulating Thin Films Materials Research Society Symposium Proceedings v 446 1997. Materials Research Society, Pittsburgh, PA, USA. 434p
Publication Year: 1997
CODEN: MRSPDH ISSN: 0272-9172
Language: English

Abstract: The proceedings contains 65 papers from the 1996 Materials Research Society Symposium on Amorphous and Crystalline Insulating thin films. Topics discussed include: insulating thin films; dielectric films; amorphous films; crystalline materials; semiconducting films; optical films; optical coatings; ULSI circuits; **dynamic random** access **memory** (**DRAM**); Ferrelectric **random** access **memory** (FRAM); **MOSFET** devices; plasma enhanced chemical vapor deposition; metallorganic chemical vapor deposition; film growth; molecular beam epitaxy; magnetron sputtering; electron cyclotron resonance; molecular dynamics; antireflection coatings; **silicon** on insulator technology; **silicon** wafers; and separation by **implantation** of oxygen (SIMOX).

33/3,AB/18 (Item 11 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04565182
E.I. No: EIP96113427048
Title: Novel pattern transfer process for bonded SOI giga-bit **DRAMs**
Author: Lee, B.H.; Bae, G.J.; Lee, K.W.; Cha, G.; Kim, W.D.; Lee, S.I.; Barge, T.; Auberton-Herve, A.J.; Lamure, J.M.
Corporate Source: SAMSUNG Electronics Co, Ltd, Kyungki-Do, South Korea
Conference Title: Proceedings of the 1996 IEEE International SOI Conference
Conference Location: Sanibel Island, FL, USA Conference Date: 19960930-19961003
E.I. Conference No.: 45625
Source: IEEE International SOI Conference 1996. IEEE, Piscataway, NJ, USA,96CH35937. p 114-115
Publication Year: 1996
CODEN: IISPED
Language: English
Abstract: **Silicon**-on-insulator (SOI) devices with buried capacitor structures have been proposed as 1 gigabit **dynamic random** access **memory** cell structure. However, wafer cost, low throughput and poor SOI thickness uniformity prevent the practical application of this technology in spite of its distinct advantages. A novel pattern transfer technology which combines hydrogen **implantation** and a selective polish top process is applied to the fabrication of a buried capacitor SOI structure. The process overcomes **most** of the drawbacks of the conventional technology. Due to the simple manufacturability and low process cost, this technology is very promising as a production technology of SOI devices with buried structures. 4 Refs.

33/3,AB/19 (Item 12 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04337789
E.I. No: EIP96013013844
Title: Isolation techniques for 256Mbit SOI **DRAM** application
Author: Hu, Yin; Houston, Ted; Rajgopal, Rajan; Joyner, Keith; Teng, Clarence
Corporate Source: Texas Instruments Inc, Dallas, TX, USA
Conference Title: Proceedings of the 1995 IEEE International SOI Conference

Conference Location: Tucson, AZ, USA Conference Date: 19951003-19951005
E.I. Conference No.: 44239
Source: IEEE International SOI Conference 1995. IEEE, Piscataway, NJ, USA,95CH35763. p 26-27
Publication Year: 1995
CODEN: IISPED
Language: English
Abstract: Various isolation techniques on SOI wafer were examined for the 256Mbit **DRAM** application. The LOCOS technique results in good isolation down to 0.6 mu m pitch, in terms of encroachment and subthreshold characteristics. The encroachment of SOI wafers is slightly better than that of bulk wafers on the thick SOI wafers and expect to be even better on the thin SOI wafers. It is the **most** efficient way to adopt LOCOS isolation for the 256Mbit SOI **DRAM** because of many years of process development experience in the bulk technology. In addition, the LOCOS isolation provides no edge leakage to the devices on SOI wafers. However, the LOCOS isolation technique may be limited as the **DRAM** cell pitch continue to scale down. (Author abstract) 2 Refs.

33/3,AB/20 (Item 13 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04305036
E.I. No: EIP95122952199
Title: MeV **implants** boost device design
Author: Voldman, Steven H.
Corporate Source: IBM, Essex Junction, VT, USA
Source: IEEE Circuits and Devices Magazine v 11 n 6 Nov 1995. p 8-16
Publication Year: 1995
CODEN: ICDMEN ISSN: 8755-3996
Language: English
Abstract: Interest in MeV **implantation** has grown as a result of the high energy technique's minimization of soft error rate, latchup, leakage, noise, and electrostatic discharge. High energy **implant** tools reduce process cost and complexity because they eliminate the need of a significant number of process steps and mask levels. Using MeV **implant** tools for retrograde wells, mask levels and process steps are eliminated. They also reduce metal contamination, thermal stress and wafer warpage. In fact, MeV **implanters** can substantially reduce the thermal budget from both processing time and temperature. MeV **implanters** also offer opportunities to eliminate **silicon** epitaxy and p plus substrates; 5-20% cost reduction have been quoted with the migration to low cost wafers and MeV technology. 22 Refs.

33/3,AB/21 (Item 14 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

04295737
E.I. No: EIP95122936007
Title: Multimedia: A new design challenge for systems-on-**silicon**
Author: Holzapfel, H.
Corporate Source: Siemens AG
Conference Title: Proceedings of the 8th International Symposium on System Synthesis
Conference Location: Cannes, Fr Conference Date: 19950913-19950915

E.I. Conference No.: 44007
Source: International Symposium on System Synthesis, Proceedings 1995. IEEE, Los Alamitos, CA, USA,PR07076. p 1
Publication Year: 1995
CODEN: 002202 ISSN: 1080-1820
Language: English
Abstract: Multimedia chips are currently the fastest growing and **most** complex consumer products in the marketplace. High performance, short development time, and low cost requirements demand a highly efficient design process. Typically, these chips are based on heterogeneous architectures composed of **embedded** DSP/RISC processors, accelerated datapaths, **embedded** (**D**)**RAM**, and analog components. In this talk, the high-level design flow of an MPEG2 single chip decoder is described, consisting of a system parser, video decoder, and audio decoder. The chip is aimed at digital TV settop boxes. Special emphasis is given to system simulation, partitioning, and architecture trade off aspects. Accelerated simulation by hardware emulation is addressed as well. (Author abstract)

33/3,AB/22 (Item 15 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

01782928
E.I. Monthly No: EI8508065187
E.I. Yearly No: EI85029694
Title: **DYNAMIC RAM** CELL STRUCTURE.
Author: Anon
Source: IBM Technical Disclosure Bulletin v 27 n 12 May 1985 p 7051-7052
Publication Year: 1985
CODEN: IBMTAA ISSN: 0018-8689
Language: ENGLISH
Abstract: This article relates generally to integrated circuit structures and more particularly to **dynamic random**-access **memory** (**DRAM**) cell construction having a stacked planar **MOS** access transistor and pn junction storage capacitor. A planar **MOS** access transistor over a buried pn junction capacitor in a **DRAM** cell requires a single **polysilicon** layer and provides improved surface topography and simplified processing steps. Because the access transistor is stacked on the capacitor, the chip area is fully used and, therefore, a very compact cell can be achieved with sufficient high storage capacitance. Because the storage capacitor is **imbedded**, all p-n junctions are available for charge storage. This provides high capacitance using a limited planar area. The surface topography is much better than the cell using double- or triple-**polysilicon** layers.

33/3,AB/23 (Item 1 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

05773754 Genuine Article#: WX055 Number of References: 130
Title: Technology challenges for integration near and below 0.1 mu m (ABSTRACT AVAILABLE)
Author(s): Asai S (REPRINT) ; Wada Y
Corporate Source: HITACHI LTD,ADV RES LAB/HATOYAMA/SAITAMA 35003/JAPAN/ (REPRINT)
Journal: PROCEEDINGS OF THE IEEE, 1997, V85, N4 (APR), P505-520

ISSN: 0018-9219 Publication date: 19970400
Publisher: IEEE-INST ELECTRICAL ELECTRONICS ENGINEERS INC, 345 E 47TH ST, NEW YORK, NY 10017-2394
Language: English Document Type: REVIEW
Abstract: Technology challenges for **silicon** integrated circuits with a design rule of 0.1 mu m and below will be addressed. We begin by reviewing the state-of-the-art CMOS technology at 0.25 mu m currently in development, covering a logic-oriented processes and **dynamic random** access **memory** (**DRAM**) processes. CMOS transistor structures are compared by introducing a figure of merit. We will then examine scaling guidelines for 0.1 mu m which has started to deviate for optimized performance from the classical theory of constant-field scaling. This will highlight the problem of nontrivial subthreshold current associated with the scaled-down CMOS with low threshold voltages. Interconnect issues are then considered to assess the performance of microprocessors in 0.1 mu m technology. It will be confirmed that 0.1 mu m technology will enable a microprocessor which runs at 1000 MHz with 500 million transistors. Challenges below 0.1 mu m will then be addressed. New transistor and circuit possibilities such as **silicon** on insulator (SOI), dynamic-threshold (DT) **MOSFET**, and back-gate-input **MOS** (BMOS) are discussed. Two **most** problems to become formidable below 0.1 mu m are highlighted. They are threshold voltage control and pattern printing. It is pointed out that the threshold voltage variations due to doping fluctuations is a limiting factor for scaling CMOS transistors for high performance. The problem with the lithography below 0.1 mu m is the low throughput for a single probe. The use of massively parallel scanning probe assemblies working over the entire wafer is suggested to overcome the problem of low throughput.

33/3,AB/24 (Item 2 from file: 34)
DIALOG(R)File 34:SciSearch(R) Cited Ref Sci

04951879 Genuine Article#: UU919 Number of References: 12
Title: IMPROVEMENT OF REFRESH CHARACTERISTICS BY SIMOX TECHNOLOGY FOR GIGA-BIT **DRAMS** (Abstract Available)
Author(s): TANIGAWA T; YOSHINO A; KOGA H; OHYA S
Corporate Source: NEC CORP LTD,MICROELECTR DEV LABS/SAGAMIHARA/KANAGAWA 229/JAPAN/
Journal: IEICE TRANSACTIONS ON ELECTRONICS, 1996, VE79C, N6 (JUN), P781-786
ISSN: 0916-8524
Language: ENGLISH Document Type: ARTICLE
Abstract: Stacked capacitor **dynamic random** access **memory** (**DRAM**) cells with both **NMOS** and **PMOS** cell transistors (Lg=0.4 mu m) were fabricated on ultra-thin SIMOX (separation by **implantation** of oxygen) substrates, and the data retention time was compared with that of a bulk counterpart. A data retention time of 550 sec (at 25 degrees C) could be achieved using ultra-thin SIMOX substrates, which is 6 times longer than that using the bulk substrate. A stacked capacitor cell with a **PMOS** cell transistor on an ultra-thin SIMOX substrate is very attractive and promising for future giga-bit **DRAM** cells.

33/3,AB/25 (Item 1 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01705461 AAD9931288
THIN DIELECTRIC TECHNOLOGY AND MEMORY DEVICES (GATE OXIDES)
Author: KING, YA-CHIN
Degree: PH.D.
Year: 1999
Corporate Source/Institution: UNIVERSITY OF CALIFORNIA, BERKELEY (0028)
Source: VOLUME 60/05-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 2265. 136 PAGES

With advances in technology and scaling, **silicon Metal-Oxide-Semiconductor** Field Effect Transistor (**MOSFET**) based VLSI circuits have remained dominant in data processing and memory applications. Perpetuated by the demand for high-performance and low-cost integrated circuits, the lateral dimensions of the **MOSFETs** are being aggressively scaled. This in turn demands scaling of the gate oxide thickness as well. Thin gate oxides present both challenges to the modeling and design device of the classical **MOSFET** and opportunities to explore new device designs and applications.

This study investigates the effect of inversion layer quantization on the capacitance and current characteristics of thin-gate-oxide **MOS** transistors. In addition, this study explores the possibility of employing thin tunnel oxide for new quasi-nonvolatile memory devices. The performance limitation of a thin dielectric floating gate memory device as well as its potential for **dynamic memory** applications are discussed. An alternative device structure (i.e. charge-trap based memory cells) is examined by the single charge tunneling model governed by Coulomb Blockade theory.

Two methods of forming charge storage nodes **embedded** in the gate dielectric are investigated. The resulting devices are then characterized. The first proposed device contains a charge trapping layer of **silicon** rich oxide (SRO) for **dynamic**/non-volatile **memory** application. This device has a similar structure as a MONOS device with SRO instead of **silicon** nitride for charge trapping on top of a very thin tunneling oxide (<2nm). Since it uses charge trapped in the oxide to create threshold voltage shift, the SRO memory cell is a non-destructive-read device. A new process of depositing SRO and high temperature oxide (HTO) in a single furnace step is developed to better top the control oxide thickness and improve data retention. This device achieved write and erase speeds comparable to that of a **DRAM** cell and longer data retention time than **DRAM**. In addition, it can be easily **embedded** into a CMOS process for low-power dynamic or quasi-nonvolatile memory applications.

Another method of **embedding** charge storage nodes into the gate dielectric employs germanium nano-crystals formed by oxidation of <math> <f> <rm>Si<inf>1-x</inf>Ge<inf>x</inf></rm></f> </math>. The device consists of a **MOSFET** with Ge nano-crystals **embedded** within the gate dielectric. This trap-formation method provides for precise control of the thicknesses of the oxide layers which sandwich the charge-traps, via thermal oxidation. Memory devices with write/erase speed/voltage and retention time superior to previously reported nano-crystal memory devices are demonstrated.

A novel method of growing multiple gate oxide thicknesses below 5nm using oxygen **implantation** is presented. Experimental results show that multiple thicknesses of gate oxide with differences of up to 20Å can be achieved on the same wafer without de gradation of the oxide interface and bulk properties. Unlike oxides grown with nitrogen **implantation**, oxides fabricated by the proposed method exhibit comparable reliability to that of thermally grown oxides.

33/3,AB/26 (Item 1 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05158511 JICST ACCESSION NUMBER: 02A0442872 FILE SEGMENT: JICST-E
SESO: Scalable Memory Using Ultra-thin Polycrystalline **Silicon**.
ISHII TOMOYUKI (1); OSABE TARO (1); MINE TOSHIYUKI (1); MURAI FUMIO (1); YANO KAZUO (1)
(1) Hitachi, Ltd., Cent. Res. Lab.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 2002, VOL.102,NO.3(ICD2002 8-15), PAGE.35-37, FIG.6, REF.9
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 681.327 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: SESO memory, which has potential to achieve low power, high density **embedded** memory without special materials, is proposed. By using ultra-thin polycrystalline **silicon** channel TFT, the leakage current becomes lower than that of standard bulk **MOS** transistor. A memory storing much lower charge than conventional **DRAM** can be operated by employing the TFT. Ultra low 1 eakage current of SESO transistor and basic operations of SESO memory are confirmed experimentally. (author abst.)

33/3,AB/27 (Item 2 from file: 94)
DIALOG(R)File 94:JICST-EPlus

05082640 JICST ACCESSION NUMBER: 02A0247623 FILE SEGMENT: JICST-E
SON-**MOSFET** using ESS technique for SoC applications.
SATO TSUTOMU (1); NII HIDEAKI (1); HATANO MASAYUKI (1); TAKENAKA KEIICHI (1); HAYASHI HISATAKA (1); HIRANO TOMOYUKI (1); IDA KAZUHIKO (1); AOKI NOBUTOSHI (1); TSUNASHIMA YOSHITAKA (1)
(1) Toshiba Corp.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 2002, VOL.101,NO.573(SDM2001 213-226), PAGE.75-80, FIG.14, TBL.1, REF.5
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: SON (**Silicon** on Nothing) **MOSFET** was successfully fabricated for the first time by using ESS (Empty Space in **Silicon**) technique as an alternative of SOI-**MOSFET**. Advantage of SON structure was experimentally demonstrated. SON structure using ESS technique is appropriate for System on a Chip (SoC) applications, such as **embedded** trench **DRAMs** and digital-analog mixed devices, due to the merit that SON structure can be fabricated partially on bulk substrate. (author abst.)

33/3,AB/28 (Item 3 from file: 94)
DIALOG(R)File 94:JICST-EPlus

04251216 JICST ACCESSION NUMBER: 99A0632250 FILE SEGMENT: JICST-E
Metal Capacitor Technology for Application to Merged **DRAM**-Logic Devices.
DRYNAN J M (1); KISHI S (1)
(1) Nec Corp.
NEC Res Dev, 1999, VOL.40,NO.3, PAGE.272-276, FIG.8, REF.5
JOURNAL NUMBER: G0138AAA ISSN NO: 0547-051X CODEN: NECRA
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Recently there has been a surge in development of **DRAM-embedded** ASICs and other System-on-a-Chip (SOC devices. Considering a high-performance CMOS process as a base into which **DRAM** is to be **embedded** or merged, it is necessary to substantially reduce the process temperatures used to fabricate storage capacitors and other structures in the **DRAM** memory cell. **Polysilicon**-Insulator-**Polysilicon** (PIP) type capacitor technology currently used in commodity **DRAMs** requires process temperatures above 75.0.DEG.C., which exceeds the 650.DEG.C. thermal budget limit of 0.18.MU.m CMOS devices. To address this process divergence, NEC has developed a Metal-Insulator-Metal (MIM) type capacitor technology, using W, Ta2O5, and TiN, that ensures **DRAM** compatibility with the surrounding on-chip logic. The process issues and specific electrical results demonstrating the feasibility of this metal capacitor technology are reported herein. (author abst.)

33/3,AB/29 (Item 4 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03482028 JICST ACCESSION NUMBER: 98A0071116 FILE SEGMENT: JICST-E
Flotation of commissioned development enterprise for "Cluster ion injection equipment for semiconductors". (Japan Science and Technology Corp. S).
Japan Sci. and Technol. Corp.
Kagaku Gijutsu Shinko Jigyodanho, 1997, NO.38, PAGE.5P
JOURNAL NUMBER: J0358BAM
UNIVERSAL DECIMAL CLASSIFICATION: 621.3:001.89 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Short Communication
MEDIA TYPE: Printed Publication

33/3,AB/30 (Item 5 from file: 94)
DIALOG(R)File 94:JICST-EPlus

03371547 JICST ACCESSION NUMBER: 97A0757882 FILE SEGMENT: JICST-E
Embedded DRAM Technology. **DRAM** merges to ASIC.
ABE KEIICHIRO (1); HASHIMOTO MASASHI (1)
(1) Nihontekisasuinsutsurumentsu

Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1997, VOL.97,NO.57(ICD97 23-30), PAGE.19-24, FIG.16, REF.3
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 681.327
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: An overview of an ASIC process technology logic based **embedded DRAM** test chip results are reported. This test chip employed 1T1C type cell. 0.5um ASIC process technology is applied. Initial **silicon** is over 80% yield without changing of process. And this chip has high speed data rate maximum 200MB/S. We confirmed that ASIC module feasibility. (author abst.)

33/3,AB/31 (Item 6 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02987933 JICST ACCESSION NUMBER: 96A0705408 FILE SEGMENT: JICST-E
A 90-MHz 16-Mb System Integrated Memory with Direct Interface to CPU.
DOSAKA K (1); YAMAZAKI A (1); WATANABE N (1); ABE H (1); OHTANI J (1); OGAWA T (1); ISHIHARA K (1); KUMANOYA M (1)
(1) Mitsubishi Electric Corp., Itami, JPN
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1996, VOL.E79-C,NO.7, PAGE.948-956, FIG.10, TBL.1, REF.5
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: This paper describes a system integrated memory with direct interface to CPU which integrates an SRAM, a **DRAM**, and control circuitry, including a tag memory (TAG). This memory realizes a computer system without glue chips, and thus enables a computer system which is low cost, low power, and compact size, but still with sufficient performance. And fast clock cycle time and access time is realized using a newly proposed clock driver and internal signal generator. This memory is fabricated with a quad-**polysilicon** double-metal 0.55-.MU.m CMOS process which is the same as used in a conventional 16-Mb **DRAM**. The chip size of 145.3 mm2 is only a 12% increase over the conventional 16-Mb **DRAM**. The maximum operating frequency is 90-MHz and the operating current at cache-hit is 156-mA. This memory is suitable for various types of computer systems such as personal digital assistants (PDA's), personal computer systems, and **embedded** controller applications. (author abst.)

33/3,AB/32 (Item 7 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02702572 JICST ACCESSION NUMBER: 96A0099971 FILE SEGMENT: JICST-E
Semiconductor Devices. System-on-**Silicon** Cell-Base IC.
SHIOCHI MASAZUMI (1); WATANABE SEIJI (1); ENKAKU MOTOHIRO (1)
(1) Toshiba Corp.

Toshiba Rebyu(Toshiba Review), 1995, VOL.50,NO.12, PAGE.879-882, FIG.6
JOURNAL NUMBER: F0360AAK ISSN NO: 0372-0462 CODEN: TORBA
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: Deep submicron technology realizes high-density and high-performance LSIs. In other words, the era of system-on-**silicon** technology, in which whole systems are integrated into only one chip, is approaching. System-on-**silicon** technology requires not only an electronic design automation(EDA) environment, but also the implementation of various megacells. Toshiba has provided a system-on-**silicon** cell-base IC(CBIC) development environment in the TC200C/TC200E series, incorporating 0.3.MU.m CMOS technology. This paper introduces the **embedded DRAM** ASIC technology, various high-performance megacells such as the RambusTM ASIC cell(RAC), and design environment of this system-on-**silicon** CBIC. (author abst.)

33/3,AB/33 (Item 8 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02679004 JICST ACCESSION NUMBER: 96A0306635 FILE SEGMENT: JICST-E
Recent developments on bonded SOI wafers.
ABE T (1); KATAYAMA M (1)
(1) Shin-Etsu Handotai, Gunma-ken
Rep Res Cent Ion Beam Technol, Hosei Univ. Suppl, 1996, NO.14, PAGE.7-15, FIG.8, TBL.2, REF.14
JOURNAL NUMBER: L0263AAM ISSN NO: 0914-2908
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication
ABSTRACT: Bonded SOI (BSOI) wafers are typically divided in two categories depending on their applications: the thick SOI and the ultra-thin SOI. The former, moreover,can be divided in to the following three thickness ranges: 1-5 .MU.m for high performance ULSI, 5-15 .MU.m for intelligent power IC's and 30-60 .MU.m for DIW (dielectric isolation wafer). **Most** of technical issues of such thick SOI (for example, layer thickness homogeneity in larger diameter wafers or defects and warpage in the case of patterned wafers) have been solved. On the other hand, the -ultra-thin SOI is expected to be applied widely for ULSI such as 1G bit **D-RAM**'s. A variety of thinning techniques to obtain homogeneous SOI layers of 0.05-0.3 .MU.m thickness has been proposed. A wafer separation method at a hydrogen **implanted** plane has recently been reported. All of the proposed methods for ultra-thin are still in a development stage. (author abst.)

33/3,AB/34 (Item 9 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02372534 JICST ACCESSION NUMBER: 95A0367012 FILE SEGMENT: JICST-E
The Double-Sided Rugged Poly Si (DSR) Technology for High Density **DRAMs**.

OGIHARA H (1); YOSHIMARU M (1); TAKASE S (1); KUROGI H (1); TAMURA H (1);
KITA A (1); ONODA H (1); INO M (1)
(1) OKI Electric Industry Co. Ltd., Hachioji-shi, JPN
IEICE Trans Electron(Inst Electron Inf Commun Eng), 1995, VOL.E78-C,NO.3,
PAGE.288-292, FIG.12, REF.4
JOURNAL NUMBER: L1370AAA ISSN NO: 0916-8524
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: The Double-Sided Rugged poly Si (DSR) technology has been developed for high density **DRAMs**. The DSR technology was achieved using transformation of rugged poly Si caused by ion **implantation** . The DSR can increase the surface area of the storage electrode, because it has rugged surfaces on both upper and lower sides. The 2-FlNs STC (STacked Capacitor cell) with DSR was fabricated in the cell size of 0.72.MU.m2, and it is confirmed that the DSR can increase the surface area 1.8 times larger than that of smooth poly Si. It is expected that 25 fF/bit is obtained with a 300 nm-thick storage electrode. These effects show that sufficient capacitance for 256 Mb **DRAMs** is obtained with a low storage electrode. It is confirmed that there is no degradation in C-V and 1-V characteristics. Moreover, the DSR needs neither complicated process steps nor special technologies. Therefore, the DSR technology is one of the **most** suitable methods for 256 Mb **DRAMs** and beyond. (author abst.)

33/3,AB/35 (Item 10 from file: 94)
DIALOG(R)File 94:JICST-EPlus

02278809 JICST ACCESSION NUMBER: 95A0235574 FILE SEGMENT: JICST-E
Technology for Processing Superminiature CMOS Transistors.
New Technol Jpn, 1995, VOL.22,NO.11, PAGE.6-7, FIG.3
JOURNAL NUMBER: X0366AAE ISSN NO: 0385-6542
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.3
LANGUAGE: English COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

33/3,AB/36 (Item 11 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01309129 JICST ACCESSION NUMBER: 91A0485923 FILE SEGMENT: JICST-E
Si ULSI. Will it reach its limits?
NATORI KENJI (1)
(1) Toshiba Corp., VLSI Res. Center
Nippon Butsuri Gakkaishi, 1991, VOL.46,NO.5, PAGE.352-359, FIG.10, REF.7
JOURNAL NUMBER: F0221AAM ISSN NO: 0029-0181 CODEN: NBGSA
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.2/.3.049.77 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

33/3,AB/37 (Item 12 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01169718 JICST ACCESSION NUMBER: 91A0076735 FILE SEGMENT: JICST-E
Intermetal dielectric planarization technology in submicron devices with spin-on-glass.
SAITO SATOSHI (1); OKAZAKI SHINGO (1); NISHIZAWA KAZUHIRA (1); SAKIYAMA KEIZO (1)
(1) Sharp Corp.
Handotai, Shuseki Kairo Gijutsu Shinpojiumu Koen Ronbunshu(Proceedings of the Symposium on Semiconductors and Integrated Circuits Technology), 1990, VOL.38th, PAGE.49-54, FIG.9, TBL.1, REF.3
JOURNAL NUMBER: F0108BAP
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2 621.382.2/.3.049.77
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Conference Proceeding
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication
ABSTRACT: In recently, multilevel metallization technology has been the subject of many investigation. Intermetal dielectrics planarization is one of the **most** important process. We have established the planarization system two yeas ago with Spin-On-Glass, CVD oxide films using TEOS and O3 gas mixture, and etchback of these films. In submicron and a half micron devices, however, CVD oxide film did not remain in narrow metal-metal space after etchback because of void formation. Therefore it is difficult to achieve the planarization of intermetal dielectrics. This paper describe the two cycles SOG process. Characteristics of SOG coating for various spaces and SOG etchback to avoid metal-metal contact failuer are key process to form milutilevel metallization. SOG was requiered to be coated flat, and SOG etchback should to be performed as the same etch rate as underlying oxide layer. Two cycles SOG process achieve the intermetal dielctrics planarization at various spaces to optimize the condition of SOG coating and etchback. In the case of 4Mbit **DRAM** apllying stacked capacitor, the oxide layer under the 1st metal is not so smooth. However, multilevel SOG layer achieved the planarization of intermetal dielectrics and good device characteristics were obtained in 4Mbit **DRAM**. (author abst.)

33/3,AB/38 (Item 13 from file: 94)
DIALOG(R)File 94:JICST-EPlus

01047778 JICST ACCESSION NUMBER: 90A0377524 FILE SEGMENT: JICST-E
Special issue : VLSI and its material. Characteristics of **silicon** required for 4-megabit and 16 megabit DRAMsGeneration alteration of LSI and materal technology.
UCHIDA MASATO (1)
(1) Toshiba Corp.
Kogyo Reametaru(Industrial Rare Metals), 1990, NO.100, PAGE.26-33, FIG.9, TBL.1
JOURNAL NUMBER: G0907AAK ISSN NO: 0368-654X CODEN: KORMA
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2 621.3:681.327.1
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary

MEDIA TYPE: Printed Publication

33/3,AB/39 (Item 14 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00841829 JICST ACCESSION NUMBER: 89A0135092 FILE SEGMENT: JICST-E
A cross section of hot-carrier phenomena in ULSIs.
TAKEDA EIJI (1)
(1) Hitachi, Ltd., Central Res. Lab.
Denshi Joho Tsushin Gakkai Gijutsu Kenkyu Hokoku(IEIC Technical Report (Institute of Electronics, Information and Communication Enginners), 1988, VOL.88,NO.276, PAGE.7-12(SDM88-103), FIG.11, TBL.2, REF.27
JOURNAL NUMBER: S0532BBG
UNIVERSAL DECIMAL CLASSIFICATION: 621.382 MIS
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Original paper
MEDIA TYPE: Printed Publication

33/3,AB/40 (Item 15 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00708595 JICST ACCESSION NUMBER: 88A0589296 FILE SEGMENT: JICST-E
Trench element separation technology for driving Al into the SiO2 film.
MIURA TAKAO (1); KASE MASATAKA (1); MATSUTANI TAKESHI (1); IMAOKA KAZUNORI (1)
(1) Fujitsu, Ltd.
Gekkan Semiconductor World(Semiconductor World), 1988, VOL.7,NO.11, PAGE.81-86, FIG.12, REF.2
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

33/3,AB/41 (Item 16 from file: 94)
DIALOG(R)File 94:JICST-EPlus

00601206 JICST ACCESSION NUMBER: 88A0261907 FILE SEGMENT: JICST-E
16M bit **dynamic RAM** technology.
FUSE HARUHIDE (1); FUKUMOTO MASAKI (1)
(1) Matsushita Electric Industrial Co., Ltd., Semiconductor Res. Center
Gekkan Semiconductor World(Semiconductor World), 1988, VOL.7,NO.4, PAGE.89-95, FIG.16, TBL.1, REF.15
JOURNAL NUMBER: Y0509AAA ISSN NO: 0286-5025
UNIVERSAL DECIMAL CLASSIFICATION: 681.327
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan
DOCUMENT TYPE: Journal
ARTICLE TYPE: Commentary
MEDIA TYPE: Printed Publication

33/3,AB/42 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal

14109315 PASCAL No.: 99-0304114
Secondary ion mass spectrometry of deep trench capacitors in **dynamic random** access **memory**
PARKS C C; GLAWISCHNIG H; LEVY M; STENGL R; DIESELDORFF Chr
IBM Analytical Services, Hopewell Junction, New York 12533; Siemens AG, Munich, Germany; IBM Burlington, Essex Junction, Vermont 05452; Siemens AG, Munich, Germany; Siemens at International Sematech, Austin, Texas 78741
Journal: Journal of vacuum science and technology. A. Vacuum, surfaces, and films, 1999-07, 17 (4) 1130-1134
Language: English
Secondary ion mass spectrometry (SIMS) supported the development of deep trench capacitors in **dynamic random** access **memory**. SIMS is done efficiently by analyzing thousands of cells in parallel and the approach described in this article is scaleable to the multi-Gbit generation. By projecting out fundamental values using geometrical formalisms, the behavior of contaminants and dopants in sub-micrometer geometries is understood without the need for small-area measurements. This array-profiling approach is used to quantify and partition halogen, alkali, and transition-metal contaminants among deep trench and other processing sectors. The deposition of self-limiting layers of arsenic during **polysilicon** fill of the deep trench is explored in detail. The doping of the trench sidewalls, either through angle ion **implants** or by drive in of doped-glass deposition, is quantified. (c) 1999 American Vacuum Society.

33/3,AB/43 (Item 2 from file: 144)
DIALOG(R)File 144:Pascal

13541806 PASCAL No.: 98-0242621
Design issues and insights for low-voltage high-density SOI **DRAM**
FOSSUM J G; CHIANG M H; HOUSTON T W
Univ of Florida, Gainesville FL, United States
Journal: IEEE Transactions on Electron Devices, 1998, 45 (5) 1055-1062
Language: English
A physics-based study of floating-body effects on the operation of SOI **DRAM** is described. The study, which is based on device and circuit simulations using a physical SOI **MOSFET** model calibrated to an actual partially-depleted (PD) SOI **DRAM** technology, addresses the performance of the peripheral circuitry, e.g., the sense amplifier, as well as the dynamic retention of the data storage cell. Design insight for low-voltage high-density SOI **DRAM** is attained. Doable cell design is shown to yield dynamic retention time long enough for gigabit memories, and crude body-source ties for **nMOS**, with **pMOS** bodies floating, are shown to effectively suppress instabilities in the sense amplifier.